Air Cavity Transmission Lines for Off-Chip Interconnects Characterized to 40 GHz

Todd J. Spencer, *Student Member, IEEE*, Rajarshi Saha, Jikai Chen, *Student Member, IEEE*, Rizwan Bashirullah, *Member, IEEE*, and Paul A. Kohl, *Member, IEEE*

***Abstract*— In this paper, air cavity transmission lines are integrated into printed circuit boards and packages to enable high-speed low-loss chip-to-chip communication. Microstripline and parallel plate structures with copper conductors separated by an air gap dielectric layer are described. The structures use a sacrificial placeholder material along with conventional microelectronics techniques to create a unique buried copper–air–copper microstripline structure. Transmission lines were characterized by *S*-parameter measurements to 40 GHz. The capacitance was tracked during fabrication to analyze the impact of the air gap. The effective dielectric constant of the final buried copper–air–copper structure was as low as 1.25.**

***Index Terms*— Air gap, interconnect, microstrip, off-chip.**

I. Introduction

POWER consumption, bandwidth, and latency in microprocessors have become critical metrics for evaluating design performance in both high-performance computing platforms and low-power mobile applications. In order to improve the power efficiencies at a given computational throughput, today's multicore designs aim to minimize energy, waste heat, and delay in electrical interconnects. Chip stacking techniques such as memory-on-die are attractive because of reduced wire length and delay. However, the number of cores and memory layers will be constrained by power delivery, via aspect ratio, wiring density, and thermal limitations [1]. Ultimately, the chip/stack must communicate with package-level components.

External links are required for chip-to-memory, chip-to-chip, and chip-to-network communications. On-chip and off-chip I/O can consume greater than half the chip power and this value is expected to increase at future technology nodes. The International Technology Roadmap for Semiconductors has singled out off-chip wires, stating, "a key bottleneck to the realization of high-performance microelectronic systems is the lack of low-latency, high-bandwidth, and high density off-chip interconnects. Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include high dielectric loss in the substrate, reflections and impedance discontinuities in the wires, and designs which are susceptible to crosstalk [2]."

Off-chip wires represent a particular challenge due to long routing distances which are orders of magnitude longer than on-chip wires. The long pathway degrades the electrical field strength, and requires higher power at the transmitter and receiver ends. Optical interconnects are superior for longer distances (tens of meters), however, they are currently not capable of replacing electrical interconnects for short and moderate distances [3]–[5]. Thus, package- and board-level electrical interconnects must have high bandwidth and should dissipate low power in the transmission media and associated circuitry.

Air gaps have been reported to have lower capacitance and reduce RC delay for on-chip interconnect applications. On-chip air gaps have been reported previously [6]–[9]. Off-chip transmission lines with air gap have also been previously reported on fiberglass-epoxy [10] and semiconductor substrates [11]–[13].

This paper expands and improves the air gap transmission lines on organic substrates reported previously [10]. Air cavity lines with a homogenous air dielectric layer fabricated using a low-residue sacrificial polymer and a higher modulus overcoat are reported. A homogenous dielectric eliminates phase offset and allows true transverse electromagnetic (TEM) operation. Both the type of photo-acid generator (PAG) (which is the primary residue after decomposition) and the PAG concentration have been minimized to reduce residue after decomposition. The higher modulus overcoat improves structural integrity and allows sacrificial decomposition with less deformation in the overcoat.

The low-loss board-level signal lines with an air cavity dielectric presented here can be used in future package generations because of the need for high-quality electrical pathways. Inclusion of an air cavity can drastically reduce capacitance and loss tangent, which are critical metrics in the evaluation of dielectric performance. Herein, we report on the fabrication and characterization of air-clad transmission lines up to 40 GHz.

II. Background

Power consumption in off-chip interconnects is best understood by analyzing loss contributions to a signal line. Two-

Manuscript received October 22, 2010; revised September 30, 2011; accepted November 26, 2011. Date of publication January 18, 2012; date of current version February 28, 2012. Recommended for publication by Associate Editor L.-T. Hwang upon evaluation of reviewers' comments.

T. J. Spencer and R. Saha are with the Department of Chemical Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: todd.spencer@chbe.gatech.edu; rajarshi.saha@chbe.gatech.edu).

J. Chen and R. Bashirullah are with the Department of Electrical Engineering, University of Florida, Gainsville, FL 32601 USA (e-mail: yfgchen@ufl.edu; rizwan@ufl.edu).

P. A. Kohl is with the Department of Chemical and Biomolecular Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0100 USA (e-mail: kohl@gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2011.2179045

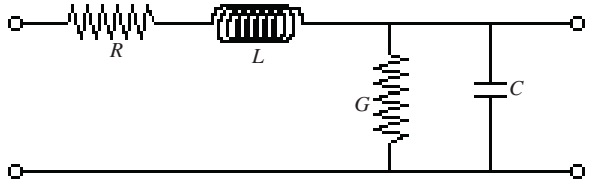

Fig. 1. Distributed element representation of transmission line structure. Resistance (R) and inductance (L) depend on conductor properties while conductance (G) and capacitance (C) depend on dielectric properties.

port S-parameters are ideal for evaluating transmission line performance because S_{21} is the ratio of the output voltage (at port 2) to the input voltage (at port 1). This is essentially the electric field decay expressed as

$$E|_{z+} = E_o e^{-\gamma \cdot l} \tag{1}$$

where E is the electric field propagating in the positive direction, E_o is the initial electric field strength, γ is the propagation constant, and l is the line length. For a fixed line length, the slope of S_{21} versus frequency is indicative of the channel quality, as it expresses the power penalty for higher frequency operation and/or wire length. While E_o and l are constrained by electrical design and physical layout, γ depends on the material properties of the transmission line.

The value of γ can be extracted using the S-parameters, with careful calibration during measurements to eliminate loss and reference plane shift from probe pads and cable [14]. The elements of the scattering matrix are converted into the propagation constant γ and the characteristic impedance Z_o. The lossy unmatched transmission line can be represented by a two-port network to solve the Telegrapher's equations, which describe the voltage and current on a transmission line. The S-parameters obtained are represented as

$$S = \frac{1}{D_s}\begin{bmatrix} \left(Z_o^2 - Z_L^2\right)\cdot \sinh \gamma l & 2Z_o Z_L \\ 2Z_o Z_L & \left(Z_o^2 - Z_L^2\right)\cdot \sinh \gamma l \end{bmatrix} \tag{2a}$$

where

$$D_s = 2Z_o Z_L \cosh \gamma l + \left(Z_o^2 - Z_L^2\right)\cdot \sinh \gamma l \tag{2b}$$

and Z_L is the termination impedance, which in this case is 50 Ω. The above matrix contains two linearly independent equations. The value of propagation constant γ and characteristic impedance Z_o for a line of length l is given by [14]

$$\gamma = \frac{1}{l}\ln \left[\frac{\left(1 - S_{11}^2 + S_{21}^2\right) \pm \sqrt{\left(1 - S_{11}^2 + S_{21}^2\right)^2 - 4S_{11}^2}}{2S_{21}}\right] \tag{3a}$$

and

$$Z_o = Z_L \sqrt{\frac{\left(1 + S_{11}^2\right)^2 - S_{21}^2}{\left(1 - S_{11}^2\right)^2 - S_{21}^2}}. \tag{3b}$$

The extracted complex propagation constant contains two solutions. The solution with the positive attenuation constant is kept and the other is ignored since it is for the wave traveling in the negative direction.

The transmission line can also be modeled by breaking it into segments and representing each segment with a lumped *RLGC* network, as shown in Fig. 1. The elements R, L, G, and C are the resistance, inductance, conductance, and capacitance per unit length and their values can be extracted from (3) using

$$R = Re\{\gamma Z_o\} \tag{4a}$$

$$L = Im\{\gamma Z_o\} \tag{4b}$$

$$G = Re\left\{\frac{\gamma}{Z_o}\right\} \tag{4c}$$

$$C = Im\left\{\frac{\gamma}{Z_o}\right\}. \tag{4d}$$

R and C in Fig. 1 models the loss due to conductor resistivity and the loss due to dielectric dissipation, respectively. At low frequencies, R is constant and is equal to the d.c. resistance. At high frequencies, however, the current flows only in a shallow band beneath the conductor surface due to skin effect, and the skin depth is inversely proportional to $\sqrt{f}$, where f is the frequency. As a result, R increases proportionally to $\sqrt{f}$ at high frequencies. In contrast, G is determined by the dielectric material's loss tangent and is proportional to f.

The complex propagation constant can also be expressed as

$$\gamma = \alpha + j\beta \tag{5}$$

where α is the attenuation constant and β is the phase constant [15]. In order to reduce losses at higher frequencies, dielectric losses must be minimized. Both the conductor loss α_c and the dielectric loss α_d have square root dependence on ε_r as

$$\alpha_c = \frac{1}{\eta \cdot d}\sqrt{\frac{2\pi \cdot f \cdot \mu_o \varepsilon_r}{2 \cdot \sigma \mu_r}} \tag{6a}$$

$$\alpha_d = \frac{\pi \cdot f}{c_o}\sqrt{\mu_r \varepsilon_r}\tan \delta \tag{6b}$$

where μ_o is the permeability of free space, ε_r is the effective relative dielectric constant, f is the frequency, σ is the conductivity of the metal, μ_0 is the permeability of free space, μ_r is the relative permeability, η is the characteristic impedance of free space (377 Ω), d is the separation distance between the signal line and its return path conductors (dielectric thickness), $\tan \delta$ is the loss tangent of the dielectric, and c_o is the speed of light in vacuum.

For microstrip lines and similar structures with nonhomogenous media, the relative dielectric constant is often described in terms of an effective dielectric constant. The effective dielectric constant accounts for different dielectric constants and is a volume-weighted mean of contributions from two or more layers of the dielectric. One key feature of microstrip lines is that the effective permittivity is lower than the relative permittivity of the dielectric because the field lines extend from the top conductor into the air before returning to ground. This feature of microstrip lines lowers the overall loss and is the key benefit of such a structure. The obvious drawback of microstrip lines is that they can only be used in the topmost layer of a substrate. A buried air cavity line has no such limitations and can benefit from a lower effective dielectric constant in multiple layers of a substrate. The frequency-dependent

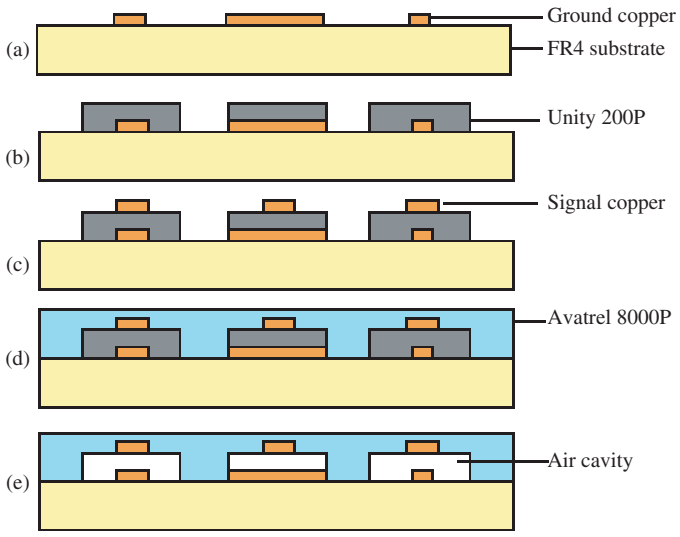

Fig. 2. Flow diagram of air-cavity line buildup process. Ground lines are patterned on an FR4 substrate.Yellow is FR4 substrate. Orange is copper. Gray is Unity 200P. Blue is Avatrel 8000P. White is air cavity.

effective relative dielectric constant ε_{eff} can be obtained from the unwrapped phase constant β [i.e., the imaginary part of the propagation constant in (5)] as

$$\varepsilon_{eff} = \left(\frac{\beta \cdot c_o}{2\pi \cdot f}\right)^2. \tag{7}$$

III. Board Fabrication Process

Transmission lines separated only by an air dielectric were fabricated on FR-4 substrates. The process flow for air cavity formation is summarized in Fig. 2. A seed layer was sputtered and electroplated through a photoresist plating mold to form the patterned ground line structures. In the second step, the sacrificial polymer was photo-patterned to define the air cavity region, as described previously [10]. Signal lines were sputtered and electroplated on top of the sacrificial polymer. The structure was encapsulated with an overcoat polymer. In the final step, the structure was heated to 220 °C, which decomposed the sacrificial material, generating the air cavity. Thus, only an air cavity separates the signal line and its return path.

The as-received substrates from Isola were preclad in 1-oz. copper (35-μm thick) on both sides of the board. The preclad copper was etched with a solution of sulfuric acid and hydrogen peroxide to remove all exposed copper. The bare substrate remained for the air cavity transmission line build-up process.

An electroplating seed layer of Ti/Cu/Ti was deposited by sputtering in a chemical vapor deposition d.c. sputtering unit. The Ti layers were added to promote adhesion of copper to the substrate (bottom Ti layer) and photoresist to the seed layer (top Ti layer). The Ti layers were 200-Å thick while the Cu layer was 500-Å thick.

The electroplating pattern for ground lines was defined by spin-coating AZ4620 photoresist to a thickness of 10 μm and photo-patterning by UV exposure at $\lambda = 365$ nm. After photoresist patterning, the Ti adhesion layer was removed with buffered oxide etch (6:1 NH_4OH:HF) to expose the copper surface for electroplating.

The ground line was electroplated in a bath of 60 g of copper sulfate, 60 ml of sulfuric acid, 1000 ml deionized water, 0.25 g of bis-sodium sulfopropyl disulfide (SPS), and 0.25 g of polyethylene glycol (molecular weight 4000 g/mol). The bath was stirred well and nitrogen was bubbled into the bottom of the bath to promote hydrogen desorption (formed during the plating process). The board surface was plated at a current density of 10 mA/cm^2 (based on the open area in the electroplating mask). A large high-purity copper anode was used as the source and an electrode was attached to the seed layer at the edge of the board. Ground lines were electroplated to a thickness of 10–12 μm as there was variation across the board surface due to the single electroplating contact. Four-point probe measurements showed the resistivity being close to that of bulk copper. After electroplating, the photoresist and seed layers were stripped.

The sacrificial polymer used was Unity2203p (Promerus LLC, Brecksville, OH), which contained poly(propylene carbonate) (PPC). It was spin-coated to a thickness of 40 μm and was sensitized with a PAG, which enabled photo-patterning [16].

The signal lines were patterned by sputtering a seed layer over the PPC, enabling a connection to the probe pads. The lines were electroplated using AZ4620 as the electroplating mask and under the same plating conditions as for the ground line. Signal line thickness varied between 10 and 12 μm in thickness on the unity polymer. Initial measurements of capacitance and loss tangent were taken at this point. At the end of each structure, the ground plane and signal line were brought onto the same plane for probing. No air cavity existed between the two at the probe pads.

The overcoat polymer was a functionalized polynorbornene, Avatrel 8000P (Promerus LLC, Brecksville, OH). The overcoat was spin-coated over the structures and photo-patterned to expose the probe pads. The influence of the overcoat on the loss tangent and capacitance was measured at this point. The final Avatrel 8000P film thickness was approximately 85 μm on the board and 60 μm over the sacrificial polymer and signal lines. The elastic modulus of the Avatrel 8000P was 3.0 GPa [17]. Compared with Avatrel 2000P used in previously reported air cavity structures [10]–[16], the higher modulus and faster cure time of 8000P allows air cavity formation without bubbling, collapse, or overcoat sagging.

In the final process step, the sample was decomposed at 220 °C in a 6-in diameter quartz tube oven purged with nitrogen at a flow rate of 10 l/min. The sample was heated at 3 °C/min to 150 °C and held for 30 min prior to ramping at 1 °C/min to 220 °C and a dwell of 2 h. The sample was cooled back to room temperature and then analyzed for capacitance, loss tangent, and *S*-parameters.

IV. Measurements and Results

Air cavity transmission lines were fabricated, electrically characterized, cross-sectioned, and imaged. Fig. 3 shows a

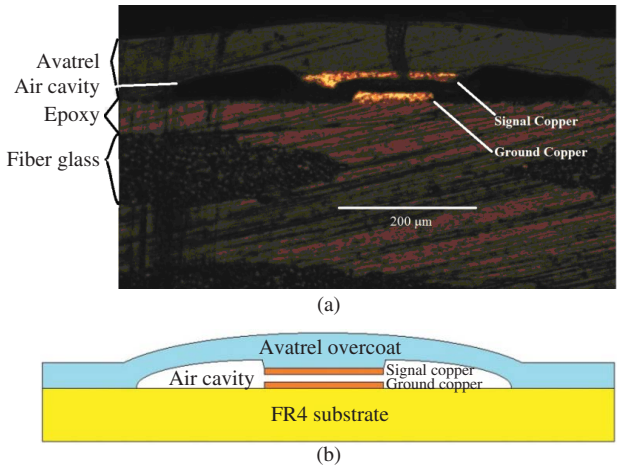

Fig. 3. (a) Labeled cross-section of 150-μm wide ground line imaged with an optical microscope. (b) Air cavity schematic.

TABLE I
CAPACITANCE MEASUREMENTS DURING PROCESSING

Line	Before overcoat (pF)	After overcoat (pF)	After sacrificial decomposition (pF)
1	6.84	9.30	6.55
2	6.93	9.11	5.82
3	6.96	9.11	5.91
4	7.09	9.21	7.75
5	7.11	9.19	7.20

All measurements taken at 100 kHz for $W = 150$ μm ground line. Line length is 5.8 cm for all lines. Lines are identical by design and are on the same board, thus any differences are due to processing variance. Before overcoat is illustrated in Fig. 2(c). After overcoat is illustrated in Fig. 2(d). After sacrificial decomposition is illustrated in Fig. 2(e).

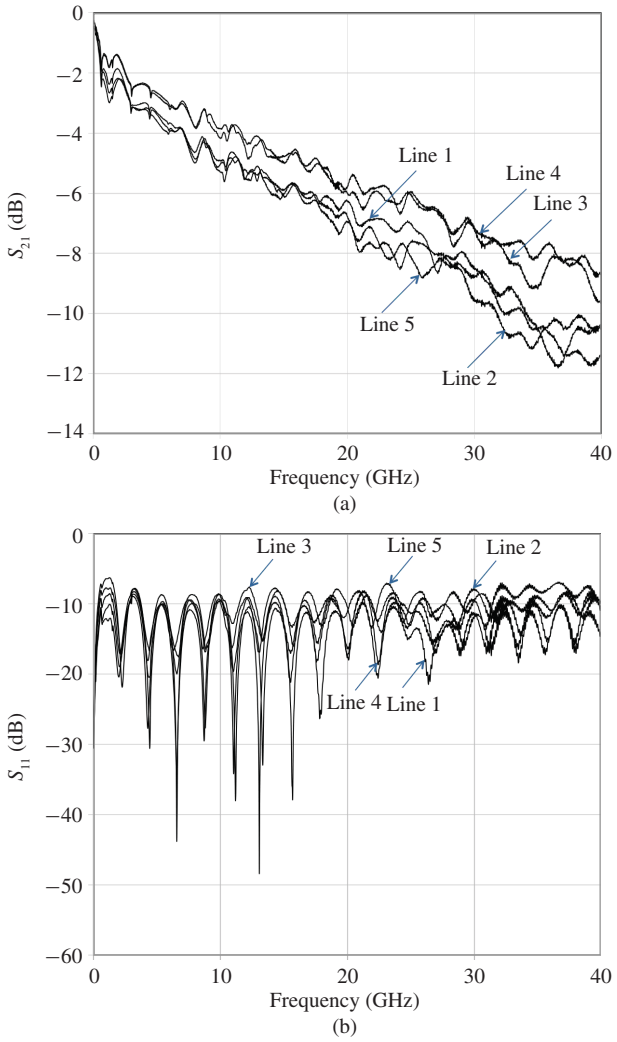

Fig. 4. (a) S_{21} measurements for 150-μm wide ground lines. (b) S_{11} measurements for 150-μm wide ground lines. Duplicate structures a–e were measured.

labeled cross-section of an air cavity line with a 150-μm wide ground line. The labeled components include the fiberglass-epoxy board, the Avatrel overcoat, the air cavity region, and the ground and signal lines. The fibers in the fiberglass board are visible along with the Avatral overcoat. The copper signal and ground lines were smooth and contiguous, but some distortion occurred in their cross section, which is due to sample preparation. Structures with different linewidths, including symmetric (same size signal and ground planes) and asymmetric signal and ground planes were fabricated.

Capacitance measurements at 100 kHz were taken at different points, during manufacture, using an HP4263A *LCR* meter with 2-μm tungsten probe tips. The capacitance between the signal and ground was measured before overcoat, after overcoat, and after decomposition of the sacrificial polymer. The measured value of capacitance is listed in Table I. The capacitance increased after the Avatrel overcoat because of the presence of Avatrel over the microstripline rather than air. After the Avatrel overcoat, the capacitance was higher, similar to that of a buried line, because it was surrounded by a higher permittivity material. Following air cavity formation, the capacitance reduced to near or below the initial value observed before overcoating with Avatrel. There was some process variability, which sometimes resulted in higher capacitance (relative to the before overcoat value) and sometimes lower capacitance in others. The process variability can be seen in Table I, where all the lines were exposed to the same processing conditions since they were on the same board. No effort was made to lower this variability, although substantial effort was previously made to control the sacrificial decomposition process by controlling the heating rate [16]. The most likely reasons for the process variation include local differences in sacrificial thickness, spatial temperature variation during heat treatments, spurious electroplating of the copper, and overcoat sagging.

The *S*-parameter values were measured using an Agilent e8363b PNA series network analyzer using Cascade Microtech ACP-50 ground–signal–ground (GSG) probes with 250-μm pitch. Data were measured from 10 MHz to 40 GHz with 25 MHz spacing over a total of 1601 scans. A shorts, opens, loads, and thrus calibration was performed prior to measurement. The measured insertion loss S_{21} for five different samples with 150-μm wide ground lines are shown in Fig. 4(a). Lines with lower capacitance show lower loss across the entire frequency range. Fig. 4(b) shows the measured values for S_{11}. Note that the resonance is due to waveguide length being equal to multiples of $\lambda/2$ at each resonant wavelength.

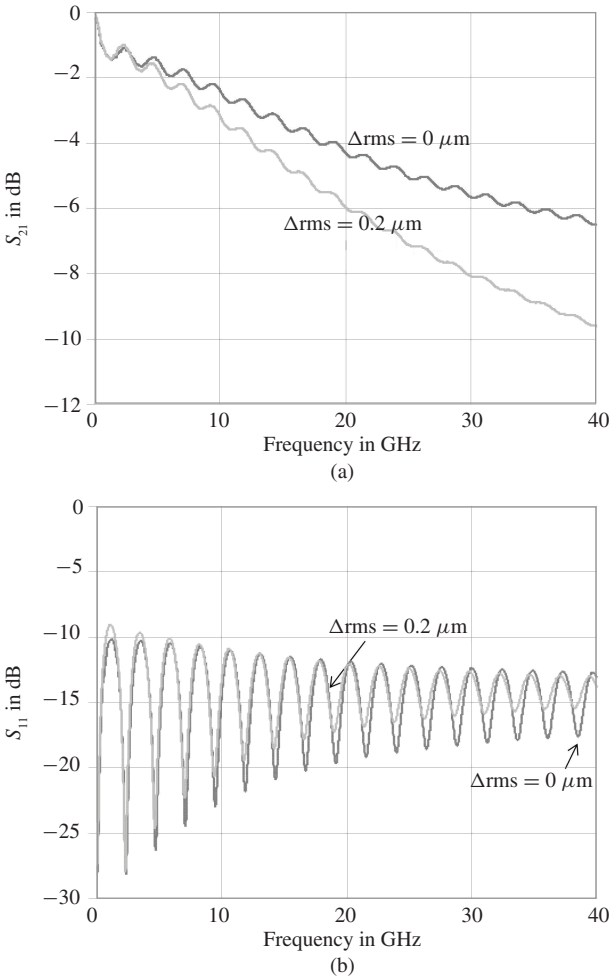

Fig. 5. (a) Simulated S_{21} characteristics of air cavity lines with 150-μm wide ground plane simulated using HFSS. Surface roughness effects for a root mean square surface roughness of 0.2 μm are also shown. (b) Simulated S_{11} characteristics of air cavity lines with 150-μm wide ground plane simulated in HFSS.

TABLE II
MATERIAL PROPERTIES USED IN SIMULATIONS

Material	ε_r	tan δ	Thickness (μm)
FR4	3.9	.015	1000
Signal Cu	—	—	12
Unity	2.28	.004	15[a]
Air	1.0006	—	15[a]
Avatrel	2.5	.009	20
Ground Cu	—	—	12

(a) Sacrificial layer thickness was simulated as 15 μm for 150-μm ground line width.

In order to investigate the impact of surface roughness on the insertion loss, frequency domain simulations were carried out using a high-frequency full-wave electromagnetic simulator (HFSS). The material properties and dimensions used in simulations are given in Table II. The simulated S_{21} and S_{11} values for the 5.8-cm line with the 150-μm wide ground plane are shown in Fig. 5(a) and (b), respectively. As shown in Fig. 4(a), the surface roughness effects for a root mean square surface roughness of 0.2 μm can account for the

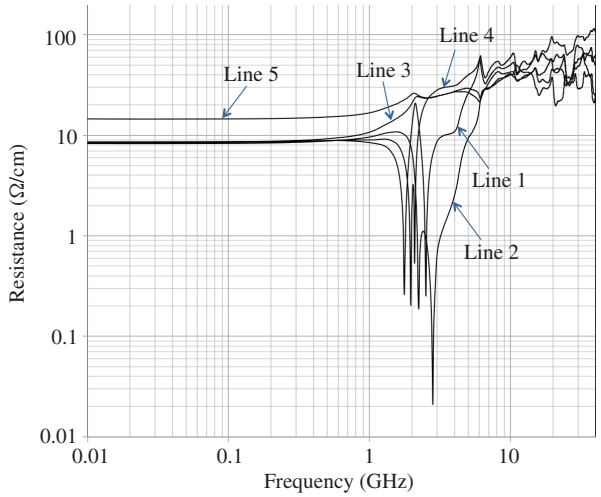

Fig. 6. Extracted resistance per unit length for 150-μm wide ground plane.

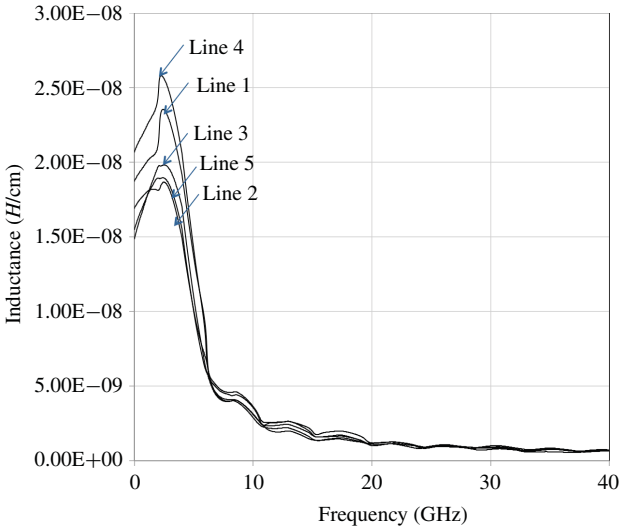

Fig. 7. Extracted inductance per unit length for 150-μm wide ground plane.

additional losses. For instance, at 20 and 40 GHz, the surface roughness increases the losses by ∼2 and ∼3.5 dB, respectively. Additional nonidealities such as probe pad effects, line defects, and variations in air gap height along the length of the line were not included. Such nonidealities are critical to line performance, as variations in height and trace width change the local characteristic impedance and have the effect of degrading line performance significantly, especially over longer trace lengths.

Another key reason for the nonideal performance may be the probe pad geometry. The probe pads were in GSG configuration with 150-μm wide pads of 250-μm length and 200-μm spacing. The signal pad transitioned to the signal line with an exponential taper that was sloped along the sidewall of the sacrificial polymer. Thus, the structure was not a true via and may have contributed to the poor return loss measurement.

The R, L, G, and C parameters were extracted from measured S-parameter data using (3) and (4), as shown in Figs. 6–9. The resistance remains constant at low frequencies and increases proportionally to $\sqrt{f}$ when the skin depth becomes comparable to the conductor size. The 150-μm wide

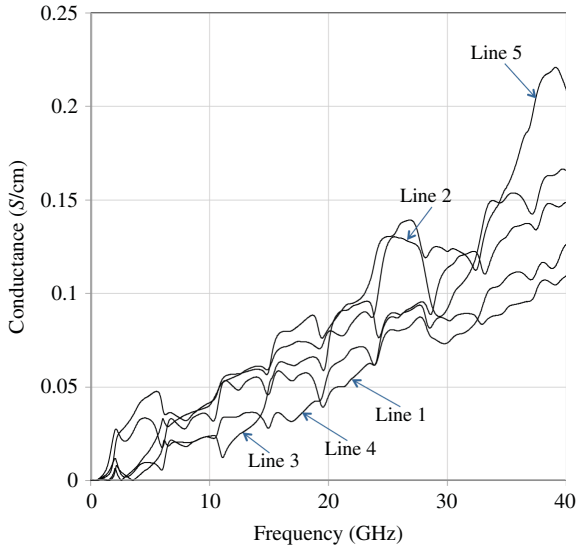

Fig. 8. Extracted conductance per unit length for 150-μm wide ground plane.

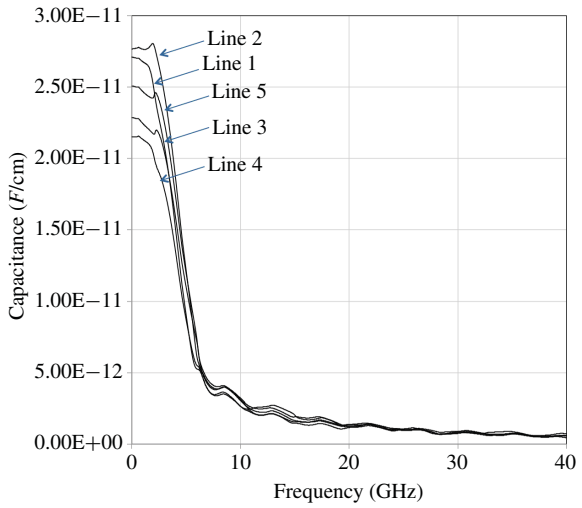

Fig. 9. Extracted capacitance per unit length for 150-μm wide ground plane.

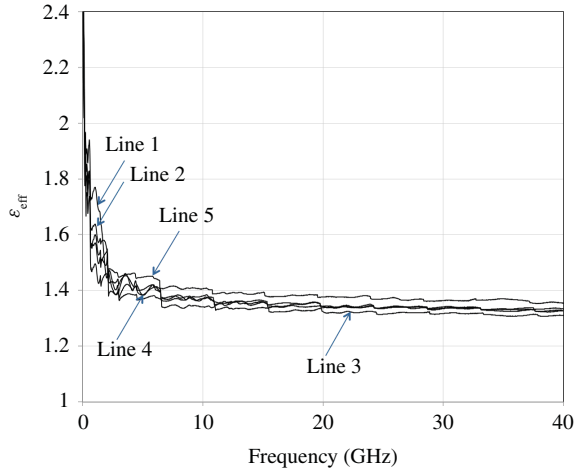

Fig. 10. Effective dielectric constant determined by unwrapped phase for 150-μm wide ground plane.

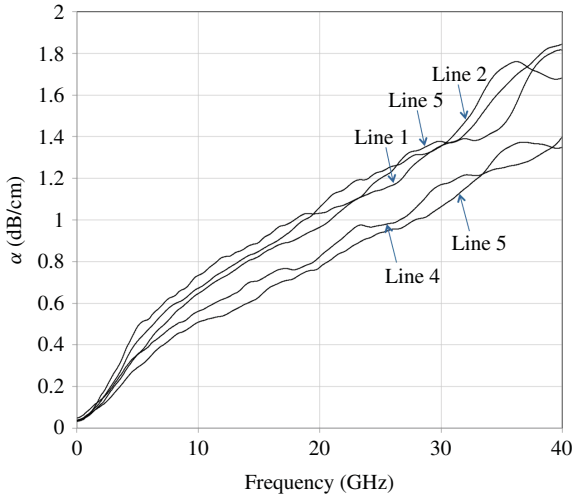

Fig. 11. Total attenuation constant per unit length for 150-μm wide ground plane.

and 5.8-cm long interconnect samples show a measured low-frequency resistance of 9–11 Ω, corresponding to an average sheet resistance of R_S ~26 mΩ/square (roughly an order of magnitude higher than that of bulk copper). The notches in the extracted resistance are likely due to measurement artifacts resulting from standing waves in the mismatched transmission line.

The extracted inductance per unit length in Fig. 7 decreases rapidly due to a reduction in magnetic field with frequency inside the conductor, gradually above 10 GHz and is relatively constantly above 20 GHz. However, the reactive effect on the signal propagation for constant inductance increases at higher frequencies. The measured conductance increases linearly with frequency and shows a non-negligible effect at microwave frequencies due to increased attenuation constant. Although an air gap is used, partial decomposition of PPC and fringing field penetration into the FR4 substrate and Avatrel overcoat can have significant contribution to dielectric losses. The extracted capacitance is higher at lower frequencies and falls off rapidly above 5 GHz, as capacitance is a direct function of the relative dielectric constant [14], [18]. In general, the reduction in capacitance can be attributed to the propagation mode changing from the slow-wave mode to a quasi-TEM mode as frequency increases [14].

The phase measurement as plotted on a Smith chart can be unwrapped by multiples of the wavelength (λ). From (7), an effective dielectric constant can be determined using the unwrapped phase of the S-parameter measurements. The effective dielectric constant, based on a line length of 5.8 cm, is plotted in Fig. 10. The measured dielectric constant for all fabricated lines is between 1.25 and 1.35, which is a significant improvement over standard transmission lines fabricated on FR-4 material. These low values of dielectric constant are impressive for a fully encapsulated copper signal wire, which indicates that the encapsulating dielectric only contributes a small portion to the overall capacitance. The total attenuation constant α as a function of frequency is plotted in Fig. 11. The value of α is extracted by taking the real part of the propagation constant, obtained using (3). The total attenuation constant for the lines at 40 GHz lies between 1.3 and 1.9 dB/cm.

V. Conclusion

Attenuation in off-chip signal wires will be a critical limitation for low-power chips with large bandwidth. Low-loss transmission lines with an air cavity dielectric offer the lowest achievable loss because of a relative permittivity near 1 and essentially zero loss tangent. The air cavity lines described in this paper exhibited low dielectric constants. The air cavity microstriplines and parallel plate lines described in this paper had effective dielectric constants below 1.5. Some uncertainty is associated with this calculation because of probe pad effects as well as surface roughness on the board and copper surface. Because the effective dielectric constant is limited by fringing fields due to geometrical layout of the line, further reduction of the dielectric constant is not seen as practical. Improved line characteristics will benefit the design of associated transmission circuitry. Better signal quality allows lower transmit powers and simpler decoding circuitry. Differential signaling can enhance data rates by offering better noise immunity and lower swing voltages and could be coupled with the high-performance air cavity lines described here. Air cavities housing multiple conductors have also been fabricated using the techniques described here. Their electrical performance has not been characterized but will be evaluated in future work.

Acknowledgment

The authors wish to thank N. Altunyurt for her assistance in *S*-parameter measurements and A. Pandey and A. Kapoor for extraction of RLGC parameters.

References

[1] D. Sekar, C. King, B. Dang, T. Spencer, H. Thacker, P. Joseph, M. Bakir, and J. Meindl, "A 3D-IC technology with integrated microchannel cooling," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Burlingame, CA, Jun. 2008, pp. 13–15.

[2] A. Allan, "International technology roadmap for semiconductors," *Semiconduct. Ind. Assoc.*, San Francisco, CA, 2009, pp. 1–23.

[3] H. Cho, K. H. Koo, P. Kapur, and K. Saraswat, "The delay, energy, and bandwidth comparisons between copper, carbon nanotube, and optical interconnects for local and global wiring application," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Burlingame, CA, 2007, pp. 135–137.

[4] J. K. Kim and C. G. Choi, "Simultaneous optical/electrical interconnection of polymer planar-lightwave-circuit chip based on polymer MOEMS and replication technology," *Sens. Actuat. A: Phys.*, vol. 126, no. 2, pp. 425–429, 2006.

[5] K. Koo, H. Cho, P. Kapur, and K. Saraswat, "Performance comparisons between carbon nanotubes, optical, and Cu for future high-performance on-chip interconnect applications," *IEEE Trans. Electron Dev.*, vol. 54, no. 12, pp. 3206–3215, Dec. 2007.

[6] S. H. Park, S. A. B. Allen, and P. A. Kohl, "Air-gaps for high-performance on-chip interconnect part I: Improvement in thermally decomposable template," *J. Electron. Mater.*, vol. 37, no. 10, pp. 1524–1533, 2008.

[7] M. B. Anand, M. Yamada, and H. Shibata, "Use of gas as low-k interlayer dielectric in LSI's: Demonstration of feasibility," *IEEE Trans. Electron Dev.*, vol. 44, no. 11, pp. 1965–1971, Nov. 1997.

[8] L. G. Gosset, V. Arnal, P. Brun, M. Broekaart, C. Monget, N. Casanova, M. Rivoire, J. C. Oberlin, and J. Torres, "Integration of SiOC air gaps in copper interconnects," *Microelectron. Eng.*, vol. 70, nos. 2–4, pp. 274–279, Nov. 2003.

[9] R. J. O. M. Hoofman, R. Caluwaerts, J. Michelon, P. H. Bernabé, J. P. Gueneau de Mussy, C. Bruynseraede, J. M. Lee, S. List, P. H. L. Bancken, and G. Beyer, "Self-aligned multi-level air gap integration," *Microelectron. Eng.*, vol. 83, nos. 11–12, pp. 2150–2154, Nov. 2006.

[10] T. J. Spencer, P. J. Joseph, T. H. Kim, M. Swaminathan, and P. A. Kohl, "Air-gap transmission lines on organic substrates for low-loss interconnects," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 9, pp. 1919–1925, Sep. 2007.

[11] H. S. Lee, "New micromachined microstrip transmission lines for application in millimeter wave circuits," *Microw. Opt. Technol. Lett.*, vol. 40, no. 1, pp. 6–9, Jan. 2004.

[12] H.-S. Lee, "Fabrication of new micromachined transmission line with dielectric posts for millimeter-wave applications," *J. Micromech. Microeng.*, vol. 14, no. 5, pp. 746–749, 2004.

[13] I. Jeong, S.-H. Shin, J.-H. Go, J.-S. Lee, C.-M. Nam, D.-W. Kim, and Y.-S. Kwon, "High-performance air-gap transmission lines and inductors for millimeter wave applications," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 12, pp. 2850–2855, Dec. 2002.

[14] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon. Hybrids Manuf. Technol.*, vol. 15, no. 4, pp. 483–490, Aug. 1992.

[15] D. M. Pozar, *Microwave Engineering*. New York: Wiley, 2005.

[16] P. J. Jayachandran, H. A. Reed, H. Zhen, L. F. Rhodes, C. L. Henderson, S. A. Bidstrup, and P. A. Kohl, "Air-channel fabrication for microelectromechanical systems via sacrificial photosensitive polycarbonates," *J. Microelectromech. Syst.*, vol. 12, no. 2, pp. 147–159, 2003.

[17] V. Rajarathinam, C. Lightsey, T. Osborn, B. Knapp, E. Elce, S. Allen, and P. A. Kohl, "Aqueous-develop, photosensitive polynorbornene dielectric: Properties and characteristics," *J. Electron. Mater.*, vol. 38, no. 6, pp. 778–786, 2009.

[18] F. Schnieder and W. Heinrich, "Model of thin-film microstrip line for circuit design," *IEEE Microw. Theory Tech. Trans.*, vol. 49, no. 1, pp. 104–110, Jan. 2001.

Todd Spencer (S'06) received the B.S. degree in chemical engineering from the University of Pittsburgh, Pittsburgh, PA, the M.S. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, and the Ph.D. degree in chemical engineering from the same institution in 2003, 2008, and 2010, respectively.

He joined Intel Assembly Test Technology Development Facility, Chandler, AZ, where he is a Packaging Engineer focused on the challenges of integrating next-generation silicon processors with high-performance packages.

Rajarshi Saha received the B.S. degree in metallurgical and materials engineering from the Indian Institute of Technology, Kharagpur, India, the M.S. degree in engineering science and the Ph.D. degree in electrical engineering both from Arizona State University, Tempe.

He has been a Post-Doctoral Researcher with the Georgia Institute of Technology, Atlanta, GA, since 2008. His current research interests include electrical connects, materials characterization, neural engineering, and microelectromechanical systems packaging.

Jikai Chen (S'11) received the B.S.E.E. degree from East China Normal University, Shanghai, China, and the M.S.E.E. degree from Zhejiang University, Hangzhou, China. He is currently pursuing the Ph.D. degree with the University of Florida, Gainesville.

He was an Analog IC Design Engineer with Realsil Microelectronics, Suzhou, China, working on PLL-based clock buffers from 2003 to 2004. From 2004 to 2006, he was a Senior Analog IC Design Engineer with Philips Semiconductors (now NXP), Eindhoven, The Netherlands, designing high-voltage LCD drivers. Since 2006, he has been a Research Assistant with the Integrated Circuit Research Laboratories, University of Florida. His current research interests include low-power circuit design for high-speed serial links.

Rizwan Bashirullah (M'99) received the B.S.E.E. degree from the University of Central Florida, Orlando, and the M.S. and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh, in 1997, 1999, and 2004, respectively.

He joined the Department of Electrical and Computer Engineering, University of Florida, Gainsville, in 2004, where he is currently an Associate Professor and the Electronics Division Area Chair. His current research interests include mixed-signal circuits for biomedical applications, power delivery systems, and on-chip/off-chip signaling subsystems.

Paul A. Kohl (M'96) received the Ph.D. degree from the University of Texas, Austin, in 1978.

He was with AT&T Bell Laboratories, Murray Hill, NJ. He joined the faculty of the Georgia Institute of Technology, Atlanta, where he is currently a Regents' Professor. He was the holder of the Thomas L. Gossage/Hercules Inc. Chair in 1989. He is the Director of the Interconnect Focus Center, one of the six Semiconductor Research Corporation Focus Centers sponsored by the Defense Advanced Research Projects Agency, Arlington, VA, and the semiconductor industry. His current research interests include electronic packaging and interconnects.