



Electroless Copper Deposition with PEG Suppression for All-Copper Flip-Chip Connections

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A fabrication technique using electroless copper deposition has been used to produce all-copper chip-to-substrate connections. This process replaces solder by electrolessly joining copper pillars on a chip and substrate. Previously, solid copper-to-copper bonding was demonstrated using a known electroless copper bath followed by low temperature annealing at 180°C for 1 h in a nitrogen environment. Although the process feasibility was demonstrated, it was inherently slow and required excessive process time. In this paper, an acceleration-suppression approach to copper plating was used to achieve a rapid deposition of high quality copper in enclosed regions. Elevated temperature was used for acceleration along with poly(ethylene glycol) (PEG) suppression. High temperature increased the transport of reactants and products in spatially restricted regions, and the addition of PEG provided control of the deposition rate. This allowed a kinetically controlled deposition while still maintaining good quality copper deposits without excessive porosity. Plating rates as high 6 $\mu\text{m}/\text{h}$ in the spatially restricted region between mated pillars were achieved. © 2009 The Electrochemical Society. [DOI: 10.1149/1.3123288] All rights reserved.

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Industry standard flip-chip connections use solder balls at the first level of packaging to make electrical connections between the integrated circuit and its substrate. Solder has many weaknesses in flip-chip applications and faces ever greater problems as the size and pitch of the solder balls shrink with device scaling. The International Technology Roadmap for Semiconductors forecasts the minimum pitch for area-array connections to shrink to 130, 100, and 90 μm in 2010, 2015, and 2020, respectively.¹ The small stand-off height accompanying fine-pitch solder balls exacerbates the problems associated with underfill materials in small gaps, which are needed with solder. Solder forms brittle copper-tin intermetallics during reflow that can compromise its thermomechanical reliability. Solder also has low electromigration resistance, which is becoming more important as the diameter of the flip-chip connections shrinks and dc power requirements increase. High aspect ratio flip-chip connections are needed for high input/output (I/O) density. Copper pillars capped with solder domes are currently used to increase the stand-off height at the first level of packaging. Copper pillars on both the chip and the substrate also move the location of the brittle copper-tin intermetallics away from the high stress region where the copper pillar (or the solder ball) intersects the chip or the substrate.

All-copper chip-to-substrate connections eliminate many of the issues with solder, underfill, and intermetallics formed between tin and copper. Copper has superior electrical conductivity and electromigration resistance vs solder. The allowable current density for electroless deposited copper is typically 10^3 greater compared to typical solder connections.^{2,3} It also has superior mechanical properties compared to solder, such as yield stress and Young's modulus. These mechanical values, along with the ability to fabricate high aspect ratio connections, can be used to form mechanically compliant interconnect structures. The elimination of underfill improves the electrical environment of the I/O signal by lowering the permittivity and loss, as well as simplifies the process flow. The flip-chip signal environment becomes increasingly important with time as the off-chip frequency continues to rise.¹ Having no tin-based materials in the I/O pathway eliminates brittle intermetallics and improves the thermomechanical reliability of the metallurgical joint. Finally, high aspect ratio, fine-pitch copper connections can be fabricated without compromising the minimum stand-off distances between the chip and the substrate. The elimination of solder, underbump metallurgy needed for solder, flux, underfill, and stripping chemicals could reduce costs and harmful environmental impacts.

Copper fusion methods have been published for wafer bonding,

but these approaches are not adequate for copper pillar bonding.^{4,5} To obtain adequate bonding between two copper surfaces, high temperature annealing (350–400°C) of “clean” copper surfaces under pressure is required.^{6,7} Organic substrate temperatures of epoxy (FR-4) or bismaleimide triazine, have an upper temperature limit of $\sim 250^\circ\text{C}$. Full-surface copper wafer bonding cannot be used for I/O because of the small surface area of pillars. Any nonuniformity between the pillars, warpage of the substrate or silicon, or nonplanarity of the chip during assembly would result in high pressure on some pillars and no contact for other pillars. Solder can accommodate a modest degree of in-plane and through-plane misalignment.

Kim et al. showed that surface-activated bonding provides a route for room-temperature copper-copper bonding.⁸ Copper-copper fusion was achieved by bonding two extremely flat and atomically clean copper surfaces in an ultrahigh vacuum environment.⁹ However, achieving atomically clean surfaces in an ultrahigh vacuum is not easily executed during chip packaging, and the process does not provide for component warpage or height variations. Solder can easily distort during reflow to elongate, flatten, or adjust for in-plane and through-plane variations.

Previously, an electroless copper plating process followed by low temperature annealing that creates copper-to-copper bonds between a chip and a substrate was reported.^{10,11} The process showed some promise as a first-level packaging solution for many reasons. First, it does not require cost-prohibitive materials or processes. There have been several reports related to gold-gold thermocompression or thermosonic bonding as a potential solder-free solution.¹²⁻¹⁴ Unfortunately, the cost of gold and the creation of metallurgical joints (i.e., not an all-copper interconnect structure) are potentially problematic.

The all-copper chip-to-substrate electroless process was able to correct for in-plane and through-plane mismatches, similar to solder.¹⁰ However, one severe disadvantage was the slow electroless deposition process (e.g., up to 18 h of plating time).¹⁰ Previous attempts to speed up the plating process by using higher temperature baths were unsuccessful, resulting in poor-quality copper and insufficient chip-to-substrate bonding.

The scope of this work is to characterize how the bonding process takes place and to reduce the electroless plating time from the previous value of 18 h. It is desirable to have a kinetically limited deposition process so that plating in small crevices between the copper pillars occurs uniformly across the package and across each pillar set. To accomplish this, an elevated temperature electroless bath was used, so that mass transfer was sufficient, along with suppression of the plating by the addition of poly(ethylene glycol) (PEG).

The effects of PEG, sulfopropyl sulfonate, and other additives on the electroless copper deposition process have been reported

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extensively.¹⁵⁻²¹ Electroless copper plating has been shown to exhibit a “superfilling” behavior analogous to the acid copper electroplating damascene process,²² using PEG as the only additive.¹⁵ The ability to plate in the highly restricted space between pillars was an important aspect of the previous publication.¹⁰ As plating occurs on the two pillars and the gap between them closes, it is very important that the two plating fronts merge together as much as possible. The merging of the copper pillars may be similar to a seamless filling of the center of a through-hole or other restricted structures where plating occurs on the sidewalls and a solid fillet is obtained with voids. Dow et al. demonstrated such a seamless filling of a through-hole by using a specific additive in the copper bath.²³ They demonstrated that additive chemistry can have a significant impact on the deposition profile over scales much closer to that used in this work (10–100 μm) vs the nanoscale trenches, which are used to test damascene plating (100 nm) applications. The goal of this work is to significantly increase the electroless deposition rate between the merging copper pillars and to retain the voidless, intimate contact obtained between the joined copper pillars.¹⁰

Experimental

Copper lines were fabricated on glass substrates to measure contact resistance between the structures during the deposition process. Copper lines were fabricated in an interdigitated comb structure with a 130 μm linewidth, a 25 μm height, and a 160 μm pitch. Once the samples were fabricated, insulated copper wiring was attached to the probe pads for electrical line-to-line measurements during plating. The resistance between the adjacent copper lines was measured while the electroless deposition process took place using a four-point probe technique. A high resolution voltmeter and ammeter were used intermittently during the electroless process to avoid disturbing the deposition.

Fabrication of the copper pillar test specimens was previously reported.¹⁰ All of the specimens used for this study used the improved photodefinable polymer collar material Avatrel 8000P.²⁴ After fabrication and temporary flip-chip attachment, the aligned samples were then placed into a copper electroless plating bath (Circuposit 3350 from Shipley Corporation). In this bath the reducing agent was formaldehyde, and the complexing agent was ethylenediaminetetraacetic acid. The pH was adjusted to 12.5 by using sodium hydroxide. To investigate the electroless inhibition by PEG, deposits were made on blank copper surfaces, and the deposition rate and surface potential were measured as a function of PEG concentration in the bath at 70°C. Copper pillars were flip-chip attached and plated for 2, 3, and 6 h at concentrations of 1, 2, and 3 ppm PEG, respectively, with stirring and nitrogen purging. The PEG was used as received from TCI Inc. with a molecular weight of 4000 g/mol.

Results

The electroless copper deposition and pillar-to-pillar bonding processes were investigated when the electrical joint was formed between the mated pillars. Experiments were performed to characterize what contributes to the copper-to-copper fusion process at moderate temperatures. The first issue addressed is the extent to which metallurgical bonds are formed between the two growing copper pillar surfaces during the electroless deposition process. Parallel copper traces were microfabricated to measure the electrical resistance between two adjacent copper lines as they grew together using the electroless copper deposition process. This test was used to investigate the presence of electrical conductivity between the lines and the impact of the annealing process on the electrical joint. Figure 1 shows the fabrication scheme and scanning electron microscopy (SEM) micrographs of the copper lines. Using a four-point probe measurement, the resistance between the isolated lines of the capacitor was measured while the sample was immersed in the electroless copper plating bath. Because the electrolyte had ionic conductivity, the resistance was measurable but large in comparison to metallic conductivity. The resistance vs deposition time for two isolated copper traces is shown in Fig. 2. As the deposition proceeds,

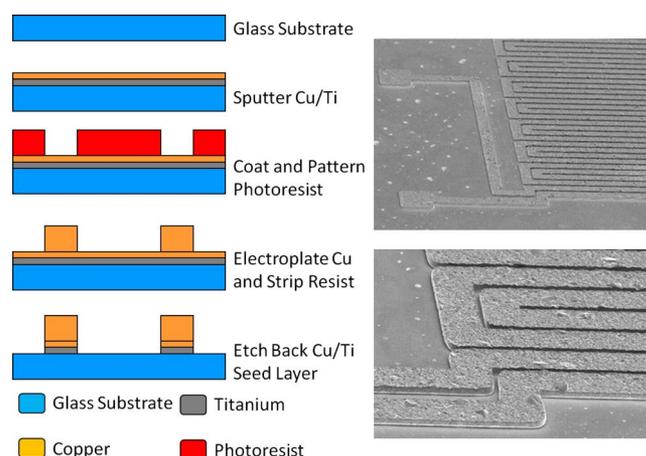


Figure 1. (Color online) (Left) Fabrication scheme for copper line capacitors. (Right) SEM images of fabricated structures.

the resistance slowly decreases as the distance (and ionic resistance) between the two copper lines decreases. Once the deposition is complete and the two metal lines touch (before annealing), the resistance is dramatically reduced. At this point (preanneal), the joint between the copper pillars is very fragile and has little mechanical strength. This result shows that metallic copper-to-copper bonding occurs after plating and that the seam between the two copper lines is closed, albeit only in isolated locations. Figure 3 shows three magnifications of a region where two copper lines merged during the electroless deposition. Under the highest magnification, an intimate metal-to-metal contact between portions of the two samples is observed.

After the samples were plated to form electrical conductivity, as shown in Fig. 1, they were annealed at 180°C for 1 h in nitrogen ambient. In previous work,⁸ this corresponds to the condition where the two pillars recrystallized and a mechanically sound joint was formed between the two structures. The resistance was measured after annealing, as shown in Table I. The electrical resistance between the two plated portions was reduced by about a factor of 10 during the annealing. This supports the concept that the copper lines (or copper pillars in the case of flip-chip bonded samples) were in limited electrical and metallurgical contact before annealing and undergo a recrystallizing process during the anneal where the grains grow together, bringing them into intimate contact to reduce or eliminate the seam.¹⁰ Optimizing the metallic bonds formed at room temperature is a promising area for future optimization. It implies

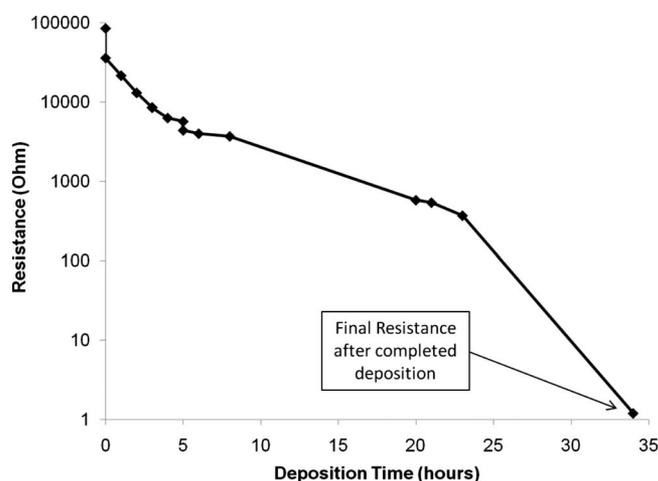


Figure 2. Resistance measure via four-point probe between copper lines during electroless deposition.

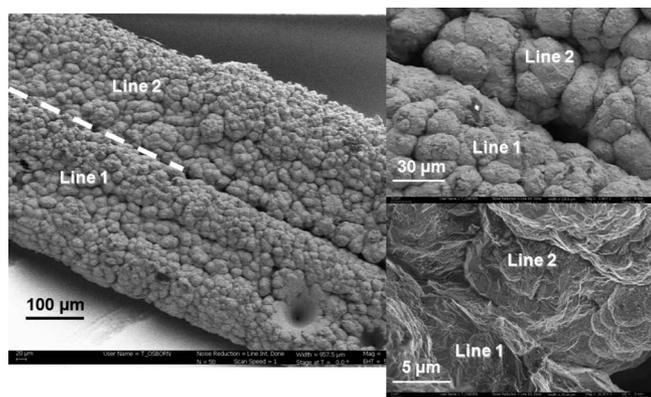


Figure 3. SEM images of the electrolessly plated lines before annealing.

that, given proper deposition conditions, seamless bonds could be formed between lines (or pillars in the case of flip-chip samples), leading to shorter or reduced temperature annealing. The seamless merging of electroplated copper surfaces also occurs in the super-filling process as part of the damascene plating. That is, the side-walls of the lines and vias are plated laterally outward and merge together without leaving a void or a metallurgical seam. Performing the same copper merging process here, on a different length scale and with minimal annealing, is highly desired.

A second goal of this work is to reduce the plating time required for a complete pillar-to-pillar bonding. Previously, long time periods were devoted to the room-temperature electroless deposition process, typically 18 h.¹⁰ Increasing the temperature increased the plating rate; however, the deposit was porous and unacceptable. There are fewer parameters to manipulate in electroless deposition, compared to electrodeposition, because current and potential cannot be externally controlled. The temperature of the electroless bath was first increased, resulting in higher deposition rates. It is common to use electroless copper processes at temperatures of 45–65°C. Unfortunately, the transport of reactants and products into the small seams between copper pillars is different from open-surface plating applications. Figure 4 illustrates the multiscale, highly constricted system for pillar-to-pillar plating. The difficulty in removing products is particularly important because the reducing agent, formaldehyde, generates hydrogen gas as a by-product, which can form bubbles between the pillars. The anodic reactions that take place on the copper surface include the hydrolysis of formaldehyde (Eq. 1), dissociation of methylene glycol (Eq. 2), dissociative adsorption (Eq. 3), charge transfer (Eq. 4), and desorption of hydrogen (Eq. 5)²⁵



Table I. Resistance of bonded Cu lines measured by four-point probe.

Sample	Resistance before annealing (mΩ)	Resistance after annealing at 180°C, 1 h (mΩ)
1	5.8	0.7
2	2.5	0.2
3	3.8	0.5

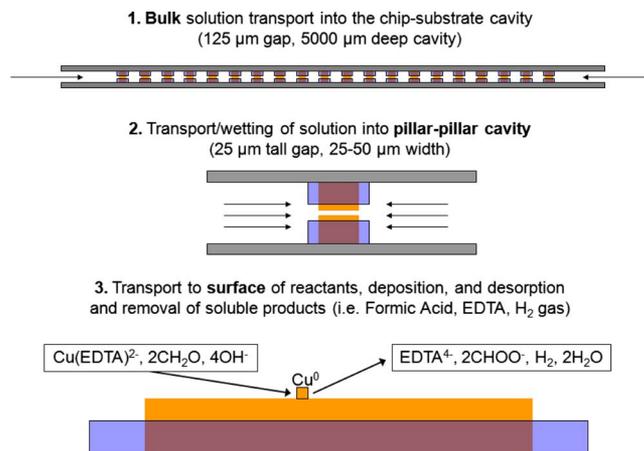


Figure 4. (Color online) Concept of the multiscale transport challenges in the all-copper flip-chip process.

If the transport of hydrogen from the surface is inadequate, gas entrapment within the spatially restricted seam can occur and lead to significant porosity in the plated metal. Figure 5 shows SEM images of the results obtained from elevated temperature plating experiments using the additive-free electroless bath. The samples plated at 45 and 65°C both showed significant porosity in the bond region. After annealing, the copper pillars were not mechanically bonded or stable.

Because increasing the temperature alone led to transport limitations and porosity, an additive-based strategy was employed. If the temperature could be increased, but the deposition rate suppressed by adsorption of an inhibitor, the kinetically controlled conditions could be maintained. PEG was chosen as an inhibiting additive because its interactions with copper surfaces and electroless plating chemistries have been studied.¹⁵⁻²¹

To characterize the effects of PEG on our electroless plating rate, various concentrations of PEG were used and the plating rate was measured. Clean copper surfaces were used for this experiment to reduce the transport limitations as much as possible. The deposition temperature was chosen to be fixed at 70°C. Figure 6 shows the results of the plating rate tests. The plating rate was dramatically reduced with only a few parts per million PEG in the bath. At 4 ppm the plating rate was near zero.

In addition to being a plating rate inhibitor in electroless copper, PEG is a leveling agent for acid copper electroplating. The leveling effects of PEG could be valuable in pillar-to-pillar plating to control the area of the pillar surfaces, which may begin to grow at rates higher than desired. In narrow trenches and restricted spaces, the diffusion of PEG may be limited and may lead to a deficiency, which would result in higher deposition rates. For example, the deposition rate measured for 0 ppm PEG was 9.05 μm/h, and the

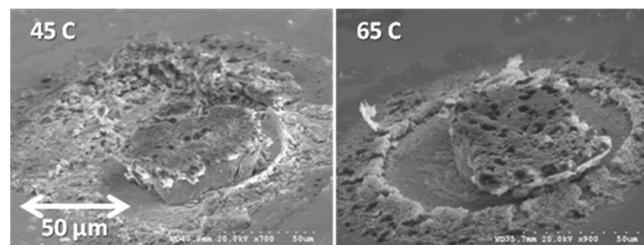


Figure 5. SEM images of results from attempting to plate at elevated temperature without additives in the bath: (Left) 45°C and (right) 65°C.

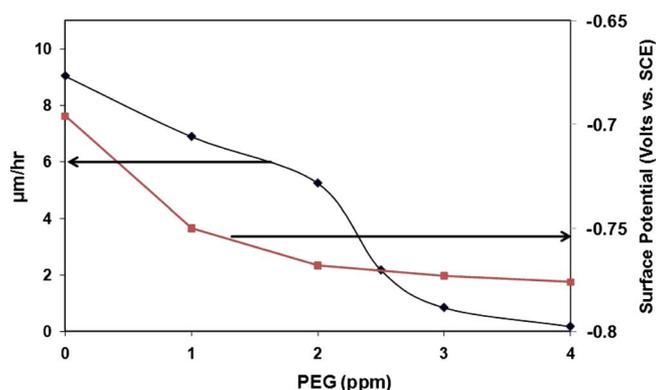


Figure 6. (Color online) Deposition rate of the electroless bath as a function of PEG concentration and the surface potential vs saturated calomel electrode.

rate at 3 ppm PEG was 0.85 $\mu\text{m}/\text{h}$. This leveling effect could lead to a greater plating rate in the restricted areas and the seamless pillar-to-pillar bonds.

Copper pillars were prefabricated on silicon substrates and were flip-chip assembled, as previously discussed.⁸ The test samples were electrolessly copper plated and joined using copper baths with different PEG concentrations. The samples were then potted in epoxy and cross sectioned before any annealing to analyze the joint between the deposited metal. Figure 7 shows the results for samples plated with 1, 2, and 3 ppm PEG at 70°C. Each sample was plated for a given time based on the separation between the pillars and the deposition rates given above. The 1, 2, and 3 ppm PEG baths were plated for 2, 3, and 6 h, respectively. The cross-section images show that the previously observed seam between the pillars is still present. However, all three samples showed no significant porosity or hydrogen bubble entrapment, as was seen from the additive-free baths. The 1 ppm PEG deposition process filled the gap in 2 h, which is a ninefold reduction in plating time compared to the original room-temperature additive-free process, which required 18 h. This is a significant reduction in plating time and brings the pillar-to-pillar bonding process to a time scale that is more comparable to solder and underfill times.

The final step was to anneal the samples and create mechanically stable joints. Using an anneal temperature of 180°C for 1 h in nitrogen ambient as reported previously,¹⁰ the joints recrystallized and formed mechanically stable pillar-to-pillar bonds. Figure 8 shows two typical cross sections for joints that were successfully bonded with the 180°C annealing process, 1 h. The interface has been removed and has formed a seamless solid copper-copper bond. It is significant that the annealing process still allows for an adequate recovery of the mechanical properties of the joint, and the copper that was deposited to fill the gap between the copper pillars recrystallized sufficiently to provide mechanical strength.

In addition to cross sections, mechanical shear tests were performed. The results for the samples plated with the 1 ppm PEG solution for 2 h and then annealed at 180°C for 1 h showed a shear

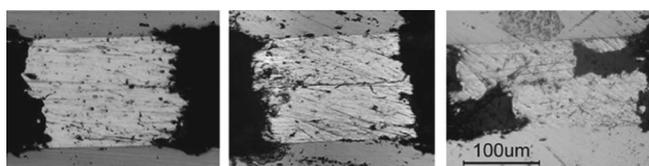


Figure 7. Cross sections after electroless deposition and before annealing: (Left) 1 ppm PEG, 2 h; (middle) 2 ppm PEG, 3 h; (right) 3 ppm PEG, 6 h.

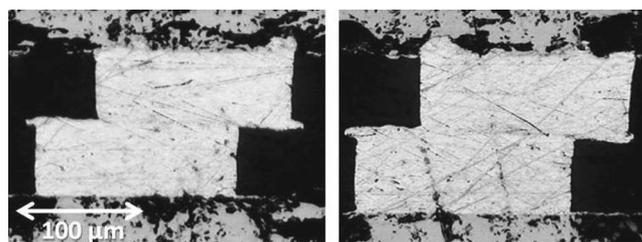


Figure 8. Cross sections of two bonds plated with 1 ppm PEG for 2 h after annealing at 180°C for 1 h.

force to break of 14.0 N. This force is directly comparable to the results we have reported previously for shear tests with the same die using the previous slow plating process.²⁶

Discussion

The deposition and bonding processes described here provide a significant reduction in the processing time for all-copper flip-chip connections. The total time for plating and annealing for a 25 μm pillar-to-pillar gap was reduced from 19 to 3 h, which includes a 1 h anneal in each case. Further reductions in the plating time could be achieved by reducing the gap between the copper pillars from 25 μm to a narrower value. For example, if the planarity of the components could be improved and the gap was reduced to as small as 5 μm , the plating process would only require 24 min. To improve the deposition rate, the critical concept was to increase the temperature to elevate both transport and kinetics but then inhibit the deposition mechanism. In this case, the inhibition was provided by the surface coverage of PEG. The net effect was to increase the plating rate from the previously described room-temperature conditions.⁸ The inhibition allowed for the transport of reactants and products onto and out of the seam between pillars so as to create solid, porosity-free copper deposits. Electrical contact between the copper pillars occurs before annealing; however, the strength of the bonded joint is not adequate until after annealing. A finer, more complete seam-filling plating process may reduce the need for annealing or lower its time and temperature. Further work on this will be pursued and may require additional additives to accelerate deposition in the seam during the last stages of plating.

Conclusion

The all-copper flip-chip plating process was improved by accelerating the plating process but keeping it in the kinetically controlled region. The inclusion of PEG in the electroless bath allowed a significant reduction in the time required to complete the bonding process, from 19 to 3 h. The experiments showed that electrically joined bonds are formed during deposition and recrystallization after the deposition completes the joining process.

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