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All-Copper Chip-to-Substrate Interconnects Part II. Modeling and Design

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A fabrication technique involving electro- and electroless copper deposition was used to produce all-copper chip-to-substrate interconnects. This process electrolessly joins copper pillars, followed by annealing at 180°C. The process is tolerant to in-plane and through-plane misalignment and height variations. The mechanical compliance and electrical performance of copper-pillar chip-to-substrate interconnects is modeled in this paper. The elastic, thermomechanical behavior and electrical performance of the chip-to-substrate interconnects are related to the geometric parameters of the pillars (pitch, diameter, and aspect ratio) and physical properties of the interconnects (yield stress, coefficient of thermal expansion, Young's modulus, Poisson's ratio, and electrical conductivity). The optimum pillar design is a trade-off between the mechanical compliance of the copper pillars and parasitic electrical effects. Copper pillars with a diameter of 48–100 μm and height of 508–657 μm are mechanically compliant and have parasitic inductance and capacitance less than 300 pH and 8.8 fF, respectively. A polymer collar improves the design space to 38–100 μm diameter and height from 441 to 617 μm.
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Mechanical reliability and electrical performance are critical issues for high-performance chip-to-substrate connections. Due to the coefficient of thermal expansion (CTE) mismatch of package materials with silicon, thermal strains and stresses are generated within the chip-to-substrate structures during chip assembly, operation, and on/off cycling.[1] For solder-based, chip-to-substrate connections, underfill is required to lower the plastic-strain accumulation at the solder bumps. The presence of underfill degrades the electrical properties of the input/output (I/O) connections and adds cost and yield loss to the assembly process. Even with underfill, thermomechanical fatigue of solder still occurs.

In this work, the use of an all-copper chip-to-substrate system connection system based on bonded copper pillars is explored. In Part I of this study, the all-copper chip-to-substrate fabrication method was described.[2] An all-copper pillar system is desirable because copper has higher conductivity and yield strength than solder. The yield strength of electrodeposited copper is approximately 225 MPa, which is higher than the ultimate strength of solders, ca. 50 MPa.[3] Copper also has elastic–plastic stress–strain characteristics. Undesired plastic deformations are generated only when the stress exceeds the yield stress of copper. Mechanical compliance can be designed into the copper pillar structures. The all-copper nature of the pillar connections avoids the formation of brittle tin–copper intermetallics which form with tin-based solders. The brittle intermetallics form fragile interfaces, often at the highest stress point in the solder-to-substrate joint (i.e., at the surface of the chip or package). Finally, unlike solder bumps, copper pillars can be made in high aspect ratio, allowing higher standoff distances for fine-pitch structures. Solder is limited to a 1:1 aspect ratio (width:height) because it goes through a melt casting. Fine pitch and short standoff distances cause flow problems for underfill in small cavities. The use of copper pillars makes it possible to maintain or increase the standoff distance as the I/O pitch shrinks.[4]

The electrical parasitics associated with integrated circuit (IC) packaging affect the performance of high-frequency ICs. In the past, the electrical role of the package was limited to providing electrical connections between the chip and other components on the substrate. However, as the switching times of transistors approach a few picoseconds and as the supply voltage scales down to less than 1 V, the electrical design of the package is becoming more challenging. Parasitic electrical effects with the package and the chip-to-substrate connections degrade the system performance by introducing signal delays, signal and power noise, and power loss. For chip-to-substrate power and ground I/O, (IR) voltage drop and simultaneous switching noise (SSN) are two main issues in distributing power to the chip. The voltage drop within the power-distribution network is due to resistance of the metal (IR drop) at each stage in the network. However, the resistance of the chip-to-substrate I/O is negligible compared to the resistance of the long, thin on-chip metallization path.[5] SSN is induced by the change in current that flows through the power-distribution network, to which the I/O inductance contributes.[6-8] SSN can cause problems in signal timing and integrity, resulting in false switching of logic circuits. Therefore, the parasitic inductance, L, of the power/ground I/O needs to be kept as low as possible in order to maintain signal integrity.

The parasitic capacitance degrades signal integrity by producing crosstalk between adjacent interconnects, resulting in signal delay that is proportional to the resistance-capacitance (RC) product. Although the absolute value of the parasitic capacitance and the resistance of chip-to-substrate I/Os are negligible compared to on-chip interconnects, the overall system performance benefits from lower off-chip RC delay.[9]

In this paper the mechanical compliance and electrical performance of coppery-pillar chip-to-substrate interconnects are analyzed in order to begin to understand the mechanical and electrical issues associated with an all-copper connection. A finite element generalized plane deformation (GPD) model using ANSYS was used to simulate the elastic, thermomechanical behavior of the copper pillars. Existing modeling approaches have been used in this study. The goal of this work is to examine the trade-off between mechanical compliance and electrical effects for copper-based, chip-to-substrate pillars. The mechanical compliance of the pillar increases with the height of the pillar (inducing less stress on the chip and substrate) at the expense of the electrical characteristics. The capacitance and inductance of the copper pillars also increases with height. The optimum design balances the mechanical and electrical effects. This paper is a first step in understanding the mechanical and electrical trade-offs for all-copper chip-to-substrate connections.

Modeling Approach

Mechanical modeling for the stress–strain relationship of the copper pillars was performed using a finite-element approach. Finite element models can be either one dimensional, two dimensional, or three dimensional (3D), modeled by lines, surfaces, or shapes, re-

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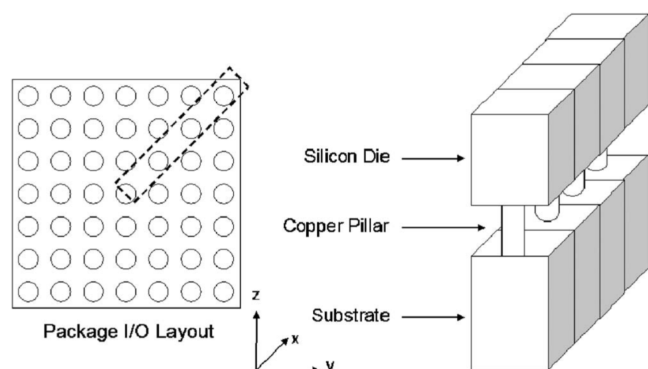

Figure 1. Illustration of GPD model.

spectively. For the stress analysis of chip-to-substrate compliant interconnects, only 3D models can be used because stress is a tensor that has both surface components and normal (vertical to the surface) components. The 3D quarter model, 3D octant model, and 3D GPD model are widely used to investigate the thermal performance and thermomechanical behavior of IC packages.[10,11] The boundary conditions in 3D quarter and octant models are either exterior surfaces or symmetry planes. Thus, the simulation results from 3D quarter and octant models are most accurate, because no simplified assumptions are made regarding the boundary conditions. However, the 3D quarter and octant models require large memory space and calculation time, making high I/O density simulation difficult. Due to the dimensional differences between the micrometer-scale copper pillars and the millimeter-scale IC and board, stress modeling of copper pillars requires an enormous number of elements to obtain convergence, especially in regions where the stress gradient is large. 3D quarter and octant models can realistically only be used when the I/O number is less than 100 with the aspect ratio less than 10 on a 4 Gb memory computer system. The technique of submodeling was developed to reduce memory space for 3D models.[12,13] Submodel simulations consist of two steps. First, a 3D quarter or octant global model containing all the structures is used to calculate the relevant properties with a coarse mesh. Although the values obtained for the fine features do not converge, the deformation of the large structures far from the region of interest (i.e., the fine structures) do converge. Then, A a submodel is constructed which contains only the regions of interest (the fine structures) and is analyzed with the boundary conditions transferred from the global model. A much finer mesh can be used with convergence in the submodel than the global model, because the physical dimensions are much smaller. However, the submodel is still limited by the maximum number of I/O that can be modeled by the global model. The International Technology Roadmap for Semiconductors (ITRS) projects the maximum number of I/O to be 3072, which would exceed the capability of a 4 Gb memory system.[14] Thus, the 3D GPD model was developed to simulate high-aspect-ratio cases without the use of extraordinary computer facilities.[15-17]

The 3D GPD model, as shown in Fig. 1, considers a diagonal slice of the package from the center of the chip along the diagonal. Figure 1 shows three I/O for illustrative purposes. The diagonal slice captures all major components, including a full set of chip-to-substrate connections. The innermost and outermost pillars along the diagonal slice (center and the corner of the chip) reflect the minimum and maximum extremes of thermal deformation. In the GPD model, the nodes on the two sides of the slice are coupled, so that all the nodes in the same plane have identical deformation in the y direction (normal to the surface). This coupling of nodes along the two planes satisfies the generalized plane-deformation constraints. Each plane is neither a free surface nor a true symmetry plane. This boundary restriction has the effect that the slice shown in Fig. 1 is free to move as a plane in the y direction, but the surface is required

Table I. Material properties used in GPD model.

	T (K)	E (GPa)	CTE (10^{-6}/K)	γ (Poisson's ratio)
BT Board	T	25.5	XY-15 Z-55	0.13
Cu	213	129.4	15.8	0.34
	298	127.7	16.6	0.34
	373	125.9	17.3	0.34
	413	125.3	17.7	0.34
	623	120	19.8	0.34
Si	213	162	1.8	0.28
	238	162	2.0	0.28
	298	162	2.5	0.28
	413	162	3.3	0.28

to remain planar.[15-17] The GPD model is a tradeoff in terms of accuracy and computational complexity, because it uses an assumed boundary condition instead of the symmetry boundary conditions. The accuracy of the analysis when used in solder-package evaluations is within 6% of the 3D octant model.[7] In this paper, a GPD model using ANSYS was used to design compliant copper-pillar chip-to-substrate interconnects that have elastic deformations for the temperature range from 25 to 125°C.

Experimental

Validation of the GPD for chip-package deformations was performed using a polymer bonded chip on a package. A layer of Avatrel 2090P (Promerus LLC, Brecksville, OH) was first spun onto a 30 mm wide square bismaleimide triazine (BT) board at a spin rate of 1000 rpm for 50 s. After being soft baked at 100°C for 10 min, a 20 mm wide square silicon chip was attached at the center. The sample was cured for 1 h at 160°C on a hotplate. The thicknesses of the chip, Avatrel layer, and BT board were 470 μm, 50 μm, and 1.18 mm, respectively. The deformation curvature of the top surface of the silicon chip was measured as heated from 25 to 98°C using a Flexus F2320. The thermally induced curvature was compared to the modeled GPD and 3D quarter chip model results.

Mechanical Analysis of Copper-Pillar Interconnects

In order for copper pillars to form a reliable connection between a low-CTE silicon IC and a high-CTE polymer-based substrate, the pillar must be able to elastically deform under the thermal stresses generated during assembly and temperature cycling during electrical activation. The ability of pillars to deform is intimately related to their aspect ratio (height-to-diameter), physical dimensions of the package (size and thickness), I/O density (number of pillars used), mechanical properties of the package, and the temperature excursion. In this study, I/O specifications from ITRS for high-performance microprocessor units have been used.[14] The chip size and I/O number are projected to be 310 mm^2 and 3072, respectively, in the year 2010. Assuming chip-to-substrate I/Os are uniformly distributed on the chip area, the I/O pitch is 318 μm. The thickness of the board and chip are estimated to be typical values of 700 and 900 μm, respectively. Thus, the number of I/O needed in the GPD model is 28, and the distance between adjacent I/Os is 452 μm. A half pillar is modeled at the center of the slide due to symmetry of the pillar at the center of the chip. The length of the slice is 12.43 mm and the width is 452 μm. The height and diameter of the copper pillars are variables in the analysis.

The mechanical properties of the materials used in the analysis for compliant copper-pillar chip-to-substrate interconnects are listed in Table I.[18-20] Temperature-dependent properties are listed in multiple rows. Selection of the criteria for maximum allowable stress is a critical input into the analysis. Exact values of acceptable I/O stress are difficult to obtain for this general analysis; however, several physical constraints must be observed. For mechanical compliance of the copper pillars, the maximum shear stress, the normal stress, and the total stress induced on copper pillars should be less than the yield stress of copper. The maximum shear stress needs to

be less than the maximum allowable adhesion stress between the copper pillars and the substrate. Physical values for adhesion strength were made and used in the analysis as minimum criteria for reliability.

The temperature excursion used to study the stress in the copper-pillar system is from 25 to 125°C, based on the typical maximum temperature achieved in Joint Electron Device Engineering Councul (JEDEC) standard accelerated thermal reliability testing.[1] The reason 25–125°C was chosen instead of −55–125°C is that the electroless copper bonding process is performed at room temperature, and as a result, the approximate neutral position of the package is at 25°C. The temperature swing from 25 to 125°C is more stringent compared to typical operating temperature swings for processor operation (typically 45–80°C) but is not as severe as other accelerated thermal reliability standards such as military standard requirements of 155°C.[1]

Electrical Analysis of Copper Pillars

The electrical performance of chip-to-substrate pillars for power and ground and signal I/O can be evaluated by considering the inductance, capacitance, resistance, and characteristic impedance of the connections, which are all functions of the pillar height, diameter, and pitch.

The formula to calculate the parasitic inductance of copper-pillar chip-to-substrate interconnects were derived for power and ground I/O, where each power (ground) I/O is surrounded by four ground (power) I/O. If each I/O carries the same amount of current, the parasitic inductance associated with a single I/O can be calculated based on a central I/O surrounded by four return I/O. Each of the four return I/O have only 25% of the area of the center I/O because they each serve as the return path for four I/O. The quarter pillars surrounding the center pillar were made cylindrical (vs quarter-cylinder structures) for simplicity. The self inductance of the quarter-cylinder pillar and cylinder pillar with the same cross-sectional area are shown to have essentially the same inductance by performing an evaluation using Raphael, an electrical analysis simulator from Technology Modeling Associates, Inc.[21,22] To perform the analysis, the copper pillar was broken into 442 identical square thin bars. The self inductance of the copper pillar was calculated based on the self inductance and mutual inductance among the discrete square bars. The simulated self inductance of a cylindrical pillar and the quarter-cylinder pillar with same cross section area are close, and the difference in inductance increases with diameter. The maximum difference is 2% for 100 μm diameter pillars. Therefore, the assumption to use round pillars with the same cross-sectional area as the quarter-round pillars is sufficiently accurate for inductance calculations.

The parasitic inductance for the center power pillar surrounded by four smaller ground pillars has been derived based on the self inductance and mutual inductance of pillar structures. The self inductance for the pillar structure (L) can be calculated by Eq. 1[22]

$$L = 0.002H\left[\ln\left(\frac{4H}{D}\right) - \frac{3}{4}\right] \times 10^{-4} \qquad [1]$$

where H is the height and D is the diameter of the pillar. The mutual inductance between two pillars (M) can be calculated by Eq. 2[23]

$$M = 0.002H\left[\ln\left(\frac{H}{d} + \sqrt{1 + \frac{H^2}{d^2}}\right) - \sqrt{1 + \frac{d^2}{H^2}} + \frac{d}{H}\right] \times 10^{-4} \qquad [2]$$

where d is the pillar pitch. For the group of pillars depicted in Fig. 2b, the four ground pillars have the same height as the center power pillar but only 1/4 the cross-sectional area; as a result, the resistance of the ground pillar is four times that of the center pillar. If no contact resistance to the pillars is assumed, the voltage drop in the circuit can be divided into that for the powered pillar and its return paths. The voltage drop, V_{circuit}, is the product of current, I, and circuit impedance, Z_{circuit}, as shown in Eq. 3. The impedance of the circuit is expressed by Eq. 4. The total circuit resistance, R_{circuit}, for the delivery and return of power is shown in Eq. 5, which would have been the same outcome regardless of the form of the return path as long as an equal cross section of metal is used for delivery and return. Substitution of Eq. 4 and 5 into Eq. 3 gives

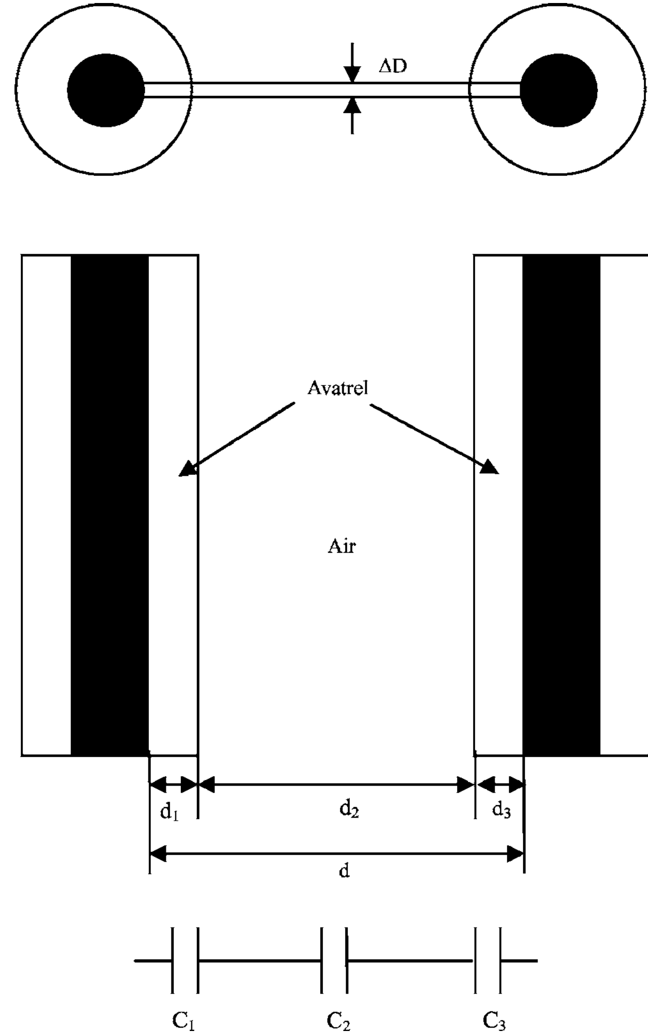

Figure 2. Illustration of the capacitance between two copper pillars with polymer collars.

$$V_{\text{circuit}} = IZ_{\text{circuit}} \qquad [3]$$

$$Z_{\text{circuit}} = R_{\text{circuit}} + j\omega L_{\text{parasitic}} \qquad [4]$$

$$R_{\text{circuit}} = R + \frac{1}{4} \cdot 4R = 2R \qquad [5]$$

$$V_{\text{circuit}} = 2IR + j\omega IL_{\text{parasitic}} \qquad [6]$$

where ω is angular frequency, j is the square root of −1, and $L_{\text{parasitic}}$ is the parasitic inductance of the power/ground I/Os.

Equation 7 is the voltage drop of the power pillar with the inductance divided between the power and return paths, Eq. 8

$$V_{\text{power}} = IR + j\omega\left(IL_{\text{power}} - 4 \cdot \frac{1}{4}IM_1\right) \qquad [7]$$

$$L_{\text{power}}^{\text{eff}} = L_{\text{power}} - 4 \cdot \frac{1}{4}M_1 \quad [8]$$

where V_{power} is the voltage drop on the power I/O, L_{power} is the self inductance of the power I/O, M_1 is the mutual inductance between the power I/O and an adjacent ground I/O, and $L_{\text{power_eff}}$ is the effective self inductance of the power I/O. The same procedure for each ground pillar gives Eq. 9, with the effective inductance of each ground pillar calculated by Eq. 10

$$V_{\text{ground}} = \frac{1}{4}I \cdot 4R + j\omega\left(\frac{1}{4}IL_{\text{ground}} + \frac{1}{4}IM_3 + 2 \cdot \frac{1}{4}IM_2 - IM_1\right) \quad [9]$$

$$L_{\text{ground_eff}} = L_{\text{ground}} + M_3 + 2M_2 - M_1 \quad [10]$$

where V_{ground} is the voltage drop on one ground I/O, L_{ground} is the self inductance of one ground I/O, $L_{\text{ground_eff}}$ is the effective inductance of one ground I/O, M_2 is the mutual inductance between the two nearest ground I/Os, and M_3 is the mutual inductance between the two ground I/Os at opposite corners among the four I/Os around the center power I/O. The voltage drop in the whole circuit is equal to the sum of the voltage drop on the power pillar and the ground pillars, as shown by Eq. 11

$$IR + j\omega\left(IL_{\text{power}} - 4 \cdot \frac{1}{4}IM_1\right) + \frac{1}{4}I \cdot 4R + j\omega\left(\frac{1}{4}IL_{\text{ground}} + \frac{1}{4}IM_3 + 2 \cdot \frac{1}{4}IM_2 - IM_1\right) = 2IR + j\omega IL_{\text{parasitic}} \quad [11]$$

After rearrangement of Eq. 11, the parasitic inductance of copper-pillar power and ground I/O can be expressed by Eq. 12

$$L_{\text{parasitic}} = L_{\text{power}} + \frac{1}{4}L_{\text{ground}} - 2M_1 + \frac{1}{2}M_2 + \frac{1}{4}M_3 \quad [12]$$

The parasitic capacitance of two chip-to-substrate copper-pillar signal I/Os can be calculated by Eq. 13 for high-frequency signals[24]

$$C = \frac{\pi\varepsilon_0\varepsilon_r}{\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]}H \quad [13]$$

where ε_0 is the permittivity of free space and ε_r is the relative permittivity.

The parasitic inductance and resistance of copper-pillar interconnects are not affected by adding polymer collars around the metal to mechanically support them. However, the parasitic capacitance increases because the polymers have a higher relative permittivity than air. The capacitance calculations for two copper pillars with collars are complex due to the distorted electrical field lines between the two circular conductors. A simple way to estimate the capacitance between the two pillars is to obtain an "effective dielectric constant" to represent the composite polymer collar and air. The polymer collar occupies a minority of the volume between the pillars, marked by ΔD in Fig. 2. The effective dielectric constant calculated based on this region is higher than the actual dielectric constant because the electrical field lines are shortest in the ΔD region in Fig. 2, and consequently, the polymer volume occupation ratio (the volume occupied by the polymer vs volume occupied by the air) is highest among all the regions between two copper pillars. The parasitic capacitance calculated base on the estimated effective dielectric constant is higher than the actual parasitic capacitance between two copper pillars. This overestimated parasitic capacitance provides a safe margin in the design space.

As shown in Fig. 2, the capacitance of the region between the two pillars is given by three series of capacitors, as shown by Eq. 14. C_1 and C_3 have equal capacitance contributions. Each capacitance was treated as a parallel plate capacitance (Eq. 15), because the electrical field lines are effectively straight. Substitution of Eq. 15 into Eq. 13 gives the effective dielectric constant as expressed in Eq. 16

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} = \frac{2}{C_1} + \frac{1}{C_2} \quad [14]$$

$$C = \frac{\varepsilon_0\varepsilon_r A}{d} \quad [15]$$

$$\varepsilon_{eff} = \frac{d\varepsilon_{\text{polymer}}}{2d_1 + d_2\varepsilon_{\text{polymer}}} \quad [16]$$

where A is the area, d_1 is the thickness of the polymer collar, and d_2 is the distance between the two polymer collar surfaces as shown in Fig. 2.

The characteristic impedance, Z_0, is defined by Eq. 17[25]

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad [17]$$

where G is the shunt conductance. For compliant copper-pillar chip-to-substrate interconnects, the shunt conductance is zero, because air is the material between the two pillars and its electrical conductivity under these conditions is zero. R can be calculated by Eq. 18, and the surface resistance, R_s, can be calculated from its definition, Eq. 19

$$R = \frac{2R_s}{\pi D}H \quad [18]$$

$$R_s = \frac{1}{\sigma\delta_s} \quad [19]$$

where σ is the conductivity of copper, which is 5.813 $\times 10^7$ (S/m), and the skin depth is defined by Eq. 20[24]

$$\delta_s = \sqrt{\frac{1}{\pi f \mu_0 \sigma}} \quad [20]$$

R_s can be expressed as a function of signal frequency in Eq. 21. Substitution of Eq. 21 into Eq. 18 gives Eq. 22

$$R_s = \frac{\sqrt{\pi f \mu_0 \sigma}}{\sigma} \quad [21]$$

$$R = 1.65906 \times 10^{-7}\frac{H}{D}f^{0.5} \quad [22]$$

L can be calculated by Eq. 23 and ωL can be calculated by Eq. 24[24]

$$L = \frac{\mu_0\mu_r}{\pi}\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]H \quad [23]$$

$$\omega L = 2.51327\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]H \times 10^{-6}f \quad [24]$$

where μ_0 is permeability of vacuum and μ_r is the relative permeability. Dividing R by ωL results in Eq. 25

$$\frac{R}{\omega L} = \frac{6.6 \times 10^{-2}}{D\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]f^{0.5}} \quad [25]$$

From the ITRS 2006 update, the chip-to-board signal frequency increases from 9.31 GHz in 2010 to 70.72 GHz by 2020.[17] Copper-pillar diameters in the range of 15–100 μm were considered. For chip-to-substrate I/Os, the pitch distance, d, is larger than D, and as a result, the natural logarithm term in Eq. 25 is larger than 1. The magnitude of the denominator of Eq. 25 is on the order of 10; this

implies that $R/\omega L$ is approximately 0.01 (much smaller than unity), which means $R \ll \omega L$. Therefore, the resistance term, R, can be neglected in Eq. 17. The characteristic impedance for copper pillars with an air dielectric can be simplified to

$$Z_0 = \sqrt{\frac{L}{C}} \quad [26]$$

Thus, the characteristic impedance of two copper pillars can be calculated by Eq. 27, which is derived by substituting of Eq. 22 and 23 into Eq. 26

$$Z_0 = \sqrt{\frac{\frac{\mu_0\mu_r}{\pi}\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]H}{\frac{\pi\varepsilon_0\varepsilon_r}{\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right]}H}} = 119.9\ln\left[\frac{d}{D} + \sqrt{\left(\frac{d}{D}\right)^2 - 1}\right] \quad [27]$$

The effect of characteristic impedance mismatch between the pillar interconnects and remainder of the wiring on the board and chip need to be evaluated because they can cause reflections and signal distortion. To analyze the effect of impedance mismatch, the load across the copper pillars was considered. The input impedance of the copper pillars with an arbitrary load impedance is calculated by Eq. 28. The return loss RL can be calculated by Eq. 29, with the reflection coefficient Γ expressed by Eq. 30[25]

$$Z_{\text{In}} = Z_0\frac{Z_L + jZ_0\tan(\beta H)}{Z_0 + jZ_L\tan(\beta H)} \quad [28]$$

$$RL = -20\log|\Gamma| \quad [29]$$

$$|\Gamma| = \left|\frac{Z_L - Z_{\text{in}}}{Z_L + Z_{\text{in}}}\right| \quad [30]$$

$$\beta = \omega\sqrt{LC} \quad [31]$$

where Z_L is the load impedance and β is the phase constant, which is defined by Eq. 31.[25]

Results and Discussion

To establish a reliable mechanical design of the copper-pillar connections, the GPD model needs to be experimentally validated for accuracy. The accuracy of the GPD model was evaluated using the polymer-attached silicon-on-BT board sample described in the Experimental section. The assembly bends concavely toward the silicon when the temperature increases because of the higher CTE of the BT board compared to the silicon. The thermal deformation was measured and simulated by the GPD model and the 3D quarter model by ANSYS for temperature excursions from 25 to 98°C. Figure 3 shows the position of the top surface (curvature) from the measurement and ANSYS simulations. The lower curve in Fig. 3 is the actual deflection, the middle is the 3D model, and the top line is the GPD model. The chip edge (right side of Fig. 3) is 10 mm away from the center point, and the 3D quarter model and GPD model are reasonably close to the true value of 32.2 μm. The deflection differences alone are not insignificant. However, the thermal deformation is a surface curve that is evaluated by the thermal-deformation strain. The thermal-deformation strain is defined as the ratio between the deflection and the distance to the neutral position (the center point). The resulting thermal-deformation strains at 10 mm from the center point are only 0.06% for the 3D quarter model and 0.13% for the GPD model off from the experimentally measured value. These results show that the GPD model is adequate for analyzing thermomechanical deformations under these conditions. The GPD model has also been previously shown to be an effective approach for approximate mechanical solutions.[7]

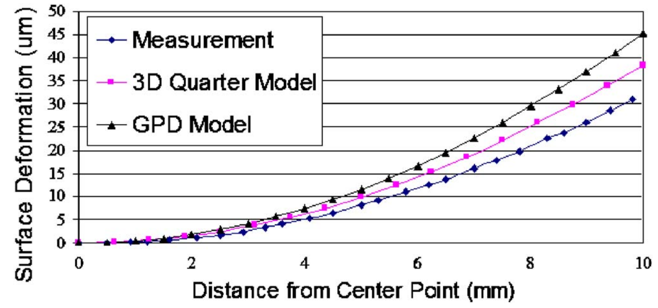

Figure 3. (Color online) Surface curvatures from experimental measurement and simulation results for 3D quarter and GPD models.

For compliant chip-to-substrate connections, the maximum stress generated needs to be lower than the yield stress of the material. Adequate mesh density needs to be used in the modeling for convergent results. For copper pillars with 30 μm diameter and 180 μm height, the maximum shear stress within the copper pillar is plotted in Fig. 4 as a function of the number of elements used in the mesh for the temperature range from 25 to 125°C. In order to avoid simulation singularity, the maximum stresses are average values among the element with the largest stress value and its adjacent elements. The results in Fig. 4 show that the shear stress does not converge until the element number exceeds 60,000 per pillar. The required mesh density depends on the stress gradient, which changes with pillar dimensions. Therefore, mesh evaluation was performed for every simulation as the pillar geometry was varied.

During thermal cycling, the maximum thermal deformation occurred at the farthest corner of the package, as shown in Fig. 5, at the location of maximum thermal stress. Figure 5 shows the thermal deformation from the GPD simulation for a 50 μm diameter, 500 μm tall copper pillars used to connect silicon onto an organic substrate (property values given in Table I). The deformation is represented by color changes from blue to red, showing the deformation from the fixed package center to the corner. The maximum stress occurs within the pillar farthest from the center of the chip at the pillar-to-board interface. The Von Mises stress distribution was obtained for the pillar farthest from the center of the chip, and the stress at the board-to-pillar interface was examined. The maximum Von Mises stress was located at the outside edge of the pillar at then substrate-to-pillar interface. This highest stress point (the outward edge at the corner farthest from the center of the chip) is sensible

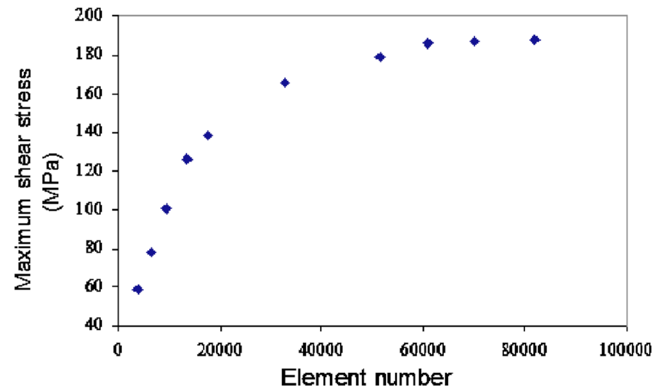

Figure 4. (Color online) Shear stress vs element number on a single copper pillar to obtain convergence.

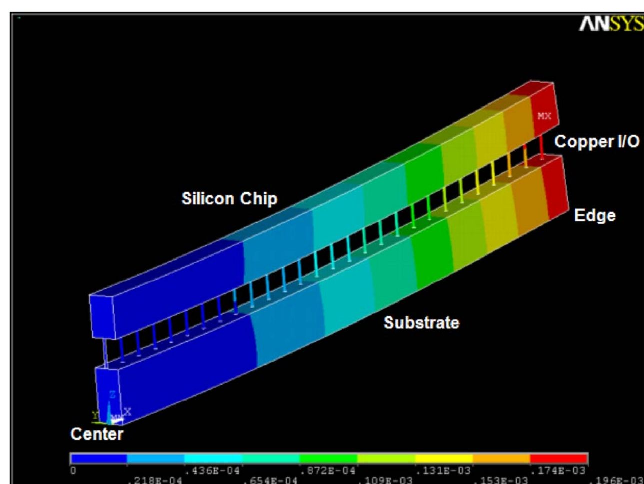

Figure 5. (Color online) Structure thermal deformation from GPD model.

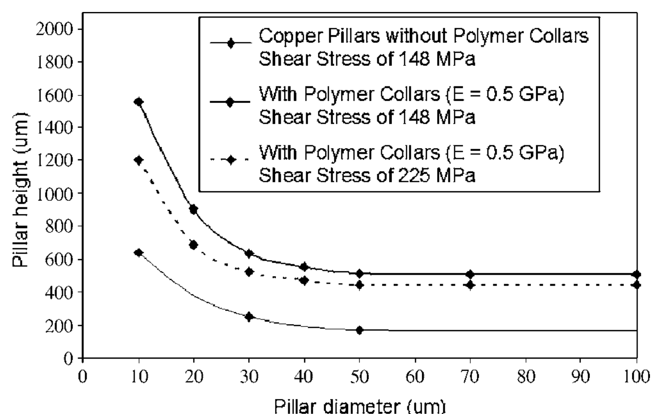

Figure 6. Mechanical compliance design space for copper-pillar chip-to-substrate interconnects.

when one considers the thermally induced curvature of the substrate due to thermal-expansion mismatch between the chip and substrate.

To be fully compliant and reliable, the chip-to-substrate copper-pillar design should have a maximum thermal stress less than the yield stress of copper. In addition, the maximum shear stress is also limited by the adhesion strength between the copper pillar and the substrate.[26] The average shear stress was measured to be 148 MPa, as presented in Part I of this study.[26] Additional and more stringent criteria may also be considered which would further limit the maximum stress at the pillar-to-substrate or pillar-to-chip interface. This includes the mechanical strength of the interlayer dielectric on the chip or chip cracking. No general criteria for these other failure modes is applied here, because such criteria are usually product and design dependent. The pillar aspect-ratio (diameter and height) limitations consistent with a maximum shear stress of about 148 MPa were investigated and are listed in Table II. The maximum normal stress and total stress on the copper pillars are also listed for each case. In each case, the maximum stress occurred at the pillar-to-board interface on the pillar at the extreme corner of the package. For each design, the normal stress increased as the diameter of copper pillars decreased, because there is less metal over which to distribute the stress. The normal stresses in all cases studied were smaller than the maximum shear stresses and less than the yield stress of copper.

In order for the pillars to be mechanically compliant, there is a minimum height for each diameter so that the stress criteria discussed above is not violated. Figure 6 shows the pillar dimensions which satisfy the maximum allowable shear stress the for adhesion criteria of 148 MPa. For 10 μm diameter copper pillars, the height needs to be taller than 1556 μm for compliant pillars. The minimum required height decreases dramatically as the diameter increases to 50 μm, after which the height reduction is small. For 50 μm diameter pillars, a height of 513 μm is sufficient to satisfy the compliance criterion. The space above the line in Fig. 6 is the region of acceptable mechanical compliance.

Lower stress was achieved in Fig. 6 by increasing the height of the pillars. There are also other ways to reduce the stress in the pillars or reduce the height while maintaining the same stress level. Polymer collars have been used around solder balls to improve their reliability in flip-chip packages.[27,28]

Polymer collars fabricated around the base of the pillar at the chip-to-substrate interface can reduce the maximum stress level by distributing the stress over a wider area.[27,28] The effect of elastic modulus of the polymer collar on the stress distribution was investigated. The mechanical properties of the three polymers ranged from 0.5 to 4.4 GPa and are listed in Table III.[29,30] The polyer used to fabricate the copper pillars in Part I of this study had an elastic modulus of 0.5 GPa, and the results are shown in Fig. 6. For Avatrel polymer collars, the simulation results show that the stress redistribution is optimized when the width of the polymer collars exceeds 15 μm and height exceeds 45 μm. The maximum stress criterion in Fig. 6 was re-evaluated using a polymer collar width of 20 μm and height of 12.5 μm less than the copper height. This leaves a 25 μm bare copper gap between the two joined copper pillars, which is one of the gaps fabricated in Part I of this study.[2] The maximum stress with a copper pillar remains at the pillar-to-board interface; however, the stress on the copper pillar is reduced for the same pillar height. The Von Mises stress distribution at the interface between the copper pillar and substrate is lower compared to the case of no polymer collar. The highest stress point at the outward edge of the pillar farthest from the center of the chip is lower because the polymer helps distribute the stress over a wider effective area. The effect on the copper aspect ratio is shown in Fig. 6. The middle dashed line is the dimension of the copper pillar with an Avatrel collar, which corresponds to a maximum shear stress of 148 MPa. The height reduction by use of the Avatrel collar is pronounced for smaller-diameter copper pillars. For the 10 μm diameter copper pillars, the required height was reduced by about 23%. As the pillar diameter

Table II. Stress results from GPD model for copper pillars without polymer collars.

Diameter (μm)	Height (μm)	Aspect ratio	Maximum shear stress (MPa)	Normal stress (MPa)	Total stress (MPa)
10	1600	160	142	100	174
20	900	45	148	51	157
30	630	21	148	39	153
40	560	14	147	34	151
50	500	10	148	19	148

Table III. Material properties of polymer collars and the shear stresses for 50 μm diameter, 500 μm tall copper pillars using polymer collars with different elastic properties.

E (GPa)	CTE (10^{-6}/K)	Poisson's ratio Γ	Maximum shear stress (MPa)	Shear stress reduction (%)
0.5	120	0.30	140	6.11
2.5	20	0.34	108	27.77
4.4	50	0.22	101	32.49

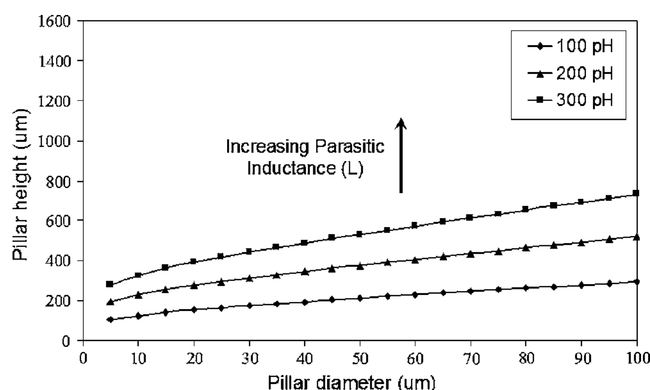

Figure 7. Parasitic inductance of power/ground I/O.

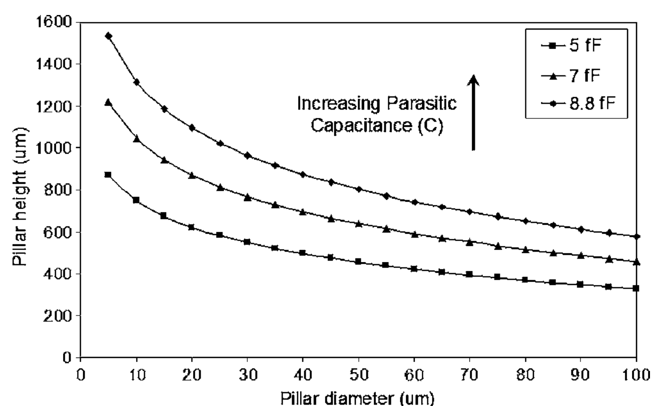

Figure 8. Parasitic capacitance of two copper pillars.

increases beyond 50 μm, the height reduction is about 13%. If the 225 MPa yield stress criteria are used, the height of the copper pillar is further reduced, as shown in Fig. 6.

The polymer collars can be made even more effective at reducing the height of the pillars if a higher-modulus polymer were used. For 50 μm diameter and 500 μm tall copper pillars, the simulation results for different polymer collars show that the maximum shear stress was reduced about 6% for a 0.5 GPa modulus collar, 28% for a 2.5 GPa modulus collar, and 32% for a 4.4 GPa modulus collar. The height needed for a 50 μm diameter copper pillar for the various polymer collars (maximum shear stress of 148 MPa) are 442, 221, and 105 μm, respectively. In terms of aspect ratio, the height-to-width of the pillars was also reduced from 10.3 for copper-only pillars to 8.8, 4.4, and 2.1 for their respective polymer collars.

The electrical performance of the copper-pillar chip-to-substrate connections is a function of the physical dimensions of copper pillars. Unlike the mechanical attributes, shorter pillars have superior electrical performance. The inductance, capacitance, and resistance can be evaluated to estimate the electrical performance of the package. The inductance causes SSN in the chip-to-substrate power-delivery network. The capacitance and resistance induce signal delay. Mismatched characteristic impedance, as determined by the inductance and capacitance, causes power loss and reflections within the signal I/O. The resistance of the chip-to-substrate copper pillar connections is small compared with on-chip resistance; therefore, only the inductance, capacitance, and characteristic impedance need to be used in the design of high-performance copper-pillar chip-to-substrate interconnect.

Flip-chip solder bumps have low parasitics due to their short height and low aspect ratio. The electrical values of solder bumps were used as a reference for evaluating the height-to-width trade-off in copper pillars. The reported inductance and capacitance values for 125 μm diameter eutectic solder bumps are 96 pH and 8.8 fF, respectively.[31] The inductance of copper pillars can be calculated from Eq. 1, 2, and 12. Figure 7 shows the dimensions for copper pillars with 96, 200, and 300 pH inductance. The inductance increases with the height of the pillars. The copper pillars with heights below the constant-inductance curves shown in Fig. 7 have lower (more desirable) values. Even the highest value here, 300 pH, is much lower than the parasitic inductance of wire-bonded packages.[32]

The capacitance of the copper pillars was calculated using Eq. 13 for pillars without polymer collars and Eq. 15 for copper pillars with Avatrel collars. Figure 8 shows the dimensions of the copper pillars which have a capacitance of 8.8, 7, and 5 fF. The region below the lines in Fig. 8 has acceptable capacitance values.

For copper pillars with polymer collars, the capacitance increases due to the higher effective dielectric constant between the two adjacent connections. The relative dielectric constant of Avatrel is 2.5.[28] The dimensions for 8.8 fF are plotted in Fig. 9. Line 9a is for copper pillars without polymer collar. Lines 9b, c, and d are for pillar dimensions with different polymer collar widths. The width of the polymer collars is 20, 30, and 40 μm for Fig. 9b-d, respectively.

The characteristic impedance of copper pillars is a function of pillar diameter and I/O pitch, as described in Eq. 27. For a 318 μm pillar pitch, the characteristic impedance has a range of 500–200 Ω for the copper pillar with the diameter of 10–100 μm, respectively. Characteristic impedances from 500 to 200 Ω are higher than the standard 50 Ω lines. Thus, the effect of impedance mismatch needs to be evaluated.

The return loss from Eq. 30 shows that the mismatch effects can be calculated from the input impedance and the standard characteristic impedance, 50 Ω. The input impedance of a copper pillar can be calculated from Eq. 28. After substituting Eq. 13, 23, and 31 into Eq. 28, the input impedance can be expressed by

$$Z_{\mathrm{in}} = Z_0 \frac{Z_\mathrm{L} + jZ_0 \tan(2.0958 \times 10^{-8} H^2 f)}{Z_0 + jZ_\mathrm{L} \tan(2.0958 \times 10^{-8} H^2 f)} \quad [32]$$

For copper-pillar chip-to-substrate interconnect, the height of the copper pillars is less than 1 mm and the signal frequency is in the range from 10 to 100 GHz. Therefore, H^2 is on the order of 10^{-6} m^2, f is on the order of 10^{10} s^{-1}, and the term $(2.0958 \times 10^{-8} H^2 f)$ is a small number; as a result, $\tan(2.0958 \times 10^{-8} H^2 f) \approx 2.0958 \times 10^{-8} H^2 f$. Using this approximation, the input impedance can be calculated by Eq. 33

$$Z_{\mathrm{in}} \approx Z_0 \frac{Z_\mathrm{L} + 2.0958 \times 10^{-8} Z_0 H^2 f j}{Z_0 + 2.0958 \times 10^{-8} Z_\mathrm{L} H^2 f j} \quad [33]$$

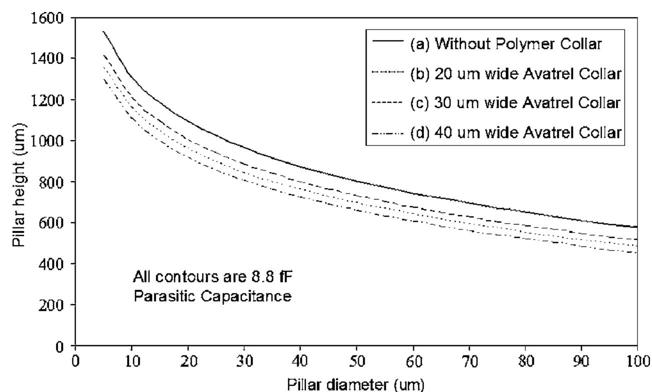

Figure 9. Capacitance values between two copper pillars: (a) no polymer collar, (b) 20 μm wide collar, (c) 30 μm wide collar, and (d) 40 μm wide collar.

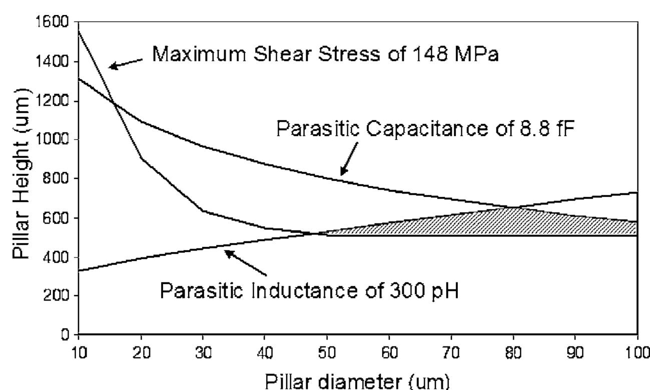

Figure 10. Combined mechanical and electrical performance design space for copper pillars without polymer collars.

Z_0 is on the order of 10^2, and Z_L is on the order of 10. The combination term of $2.0958 \times 10\%ZH^2fj$ is on the order of 10^{-2}, which is 3 to 4 orders of magnitude smaller than Z_0 and Z_L. Therefore, the $2.0958 \times 10^{-8}ZH^2fj$ term in Eq. 33 can be neglected. This means that the input impedance is equal to the load impedance, as shown by Eq. 34

$$Z_{in} \approx Z_0\frac{Z_L}{Z_0} = Z_L \qquad [34]$$

The result in Eq. 34 shows that although the characteristic impedance of the chip-to-substrate copper pillars is high (200–500 Ω), it does not affect the impedance of the signal lines because they are short (less than 1 mm). The reflection coefficient between the copper pillar connected to the chip and the board is negligible, and, as a result, there is no return loss for chip-to-substrate copper-pillar connections.

The results in the previous sections can be combined so as to consider the overlap in the mechanical and electrical design space. Figure 10 shows the design curves for copper pillars without polymer collars. The upper region is mechanically compliant for the criteria of maximum shear stress less than 148 MPa. The region below the middle line has a capacitance less than 8.8 fF. The region below the bottom line has an inductance less than 300 pH. The overlap region, as identified by the slashed lines, satisfies all three requirements. This region covers pillar diameters from 48 to 100 μm with heights from 508 to 657 μm. Copper pillars with dimensions in this region are low in electrical parasitics and sufficiently compliant.

The design space for copper pillars with 20 μm wide low modulus polymer collars is plotted in Fig. 11. Compared with Fig. 10, the mechanically compliant curve and capacitance curve move downward, while the inductance curve remains unchanged. The overlap region that satisfies all the requirements is larger than in Fig. 10, because the mechanical improvement of the polymer collar is more significant than the capacitive electrical penalty. The optimum design space covers pillar diameters from 38 to 100 μm with heights from 441 to 617 μm. Copper pillars with Avatrel collars with dimensions in this region are compliant and have low electrical parasitic characteristics.

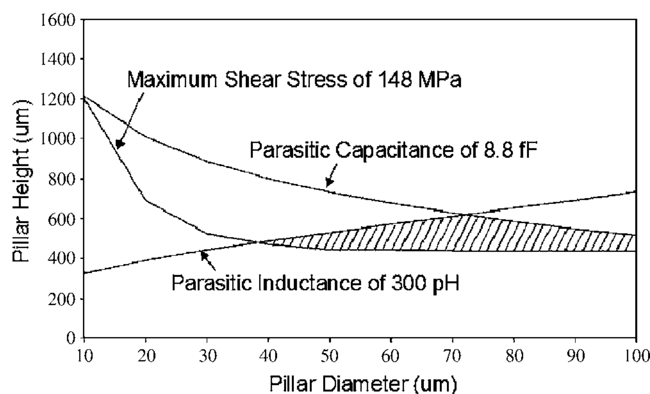

Figure 11. Combined mechanical and electrical performance design space for copper pillars with Avatrel polymer collars.

The ultimate design space for chip-to-substrate connections can be changed by considering other factors, both positive and negative. More stringent requirements, such as lower stress and lower capacitance or inductance have already been discussed. The design space can also be expanded by considering alternate designs and materials. A stiffer polymer collar can expand the design space by reducing the highest stress value in the copper pillar. The benefits of a higher modulus polymer occur as long as its molulus is less than that of copper. Alternatively, the area–array of copper pillars considered here can be altered. Lower stress could occur if the pillars were gathered in a tighter array and not located at the extreme corners of the chip. One could also change the diameter of the pillars as a function of position on the chip. It is also advantageous to change the shape of the chip-to-substrate connections because the I/O are no longer required to be circular due to round solder balls. Noncircular pillars (oval or rectangular) would redistribute the stress from the highest point (at the edge of the cylindrical I/O) over a wider front and lower the maximum stress value. Analysis of these scenarios could expand the resulting design space.

Conclusions

In this paper, the mechanical and electrical performance of copper-pillar chip-to-substrate interconnects are discussed. A finite-element GPD model was employed to design fully compliant copper pillars, reducing the need for underfill. The electrical parasitics of copper-pillar chip-to-substrate interconnects were studied. There is a trade-off between mechanical and electrical benefits in the copper-pillar geometry. Higher aspect ratio reduces the mechanical stresses generated on the pillars, which improves the reliability of the whole package. However, the increased aspect ratio also induces higher electrical parasitics. In conclusion, without the presence of polymer-supporting collars, copper pillars with the dimension of diameter from 48 to 100 μm and height from 508 to 657 μm are mechanically compliant and have parasitic inductance and capacitance less than 300 pH and 8.8 fF, respectively. With the presence of Avatrel polymer collars at both ends of the copper pillars, the dimension space for compliant high-performance copper pillars is enlarged to have diameters from 38 to 100 μm with heights from 441 to 617 μm. The aspect ratio required for compliant copper-pillar interconnects can be further reduced by either improvement of the adhesion strength between copper pillars with the substrate or using higher elastic modulus polymer collar materials.

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List of Symbols

ΔV voltage noise, V
L inductance, H, or length, m
I current, A
t time, s
V_{dd} supply voltage, V
τ shear stress, Pa

F force, N
A cross-sectional area or area, m^2
T temperature, K
E elastic modulus, Pa
γ Poisson's ratio or thermal deformation strain
ΔH thermal deformation, m
H height, m
D diameter, m
d pitch or distance, m
V voltage, V
Z impedance, Ω
R resistance, Ω
ω angular frequency, Hz
j imaginary unit, square root of -1
M mutual inductance, H
f signal frequency, Hz
C capacitance, F
G conductance, S
ε_0 permittivity of vacuum
ε_r relative dielectric constant (relative permittivity)
μ_0 permeability of vacuum
μ_r relative permeability
ε'' imaginary part of the complex permittivity
R_s surface resistance, Ω
Z_0 characteristic impedance, Ω
σ conductivity, S/m
δ_s skin depth, m
Z_L load impedance, Ω
β phase constant, rad/m
ρ electrical resistivity, Ωm
ΔD infinite small distance, m
S stiffness, N/m
P force, N
E_r reduced modulus, Pa
h displacement, m

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