



## All-Copper Chip-to-Substrate Interconnects Part I. Fabrication and Characterization

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A fabrication process has been developed and characterized to create all-copper chip-to-substrate input/output connections. Electroless copper plating followed by low-temperature annealing in a nitrogen environment was used to create an all-copper bond between copper pillars. The ability to fuse the two copper surfaces at modest temperature and pressure is demonstrated. The bond strength for the all-copper structure exceeded 165 MPa after annealing at 180°C. During the anneal process, a significant microstructural transformation in the bonded copper-copper interface was observed. The changes were correlated to an increase in the bond strength. The process was characterized with respect to in-plane misalignment of bond sites. Significant planar misalignment, greater than the diameter of the pillars, could be tolerated. Through-plane mismatches between the pillars (pillar gap) as large as 65 μm could be overcome, resulting in good pillar-to-pillar bonding. Successful silicon-on-silicon and silicon-on-FR-4 bonding was achieved with no degradation of the organic board.

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Flip-chip interconnects use solder balls to make electrical connections between the integrated circuit chip and its substrate. Solder has many disadvantages in this application, and they are becoming more restrictive as the interconnect size continues to shrink to meet the input/output (I/O) demands of high-performance components. The International Technology Roadmap for Semiconductors forecasts minimum pitch for area array interconnects to shrink to 120, 100, and 85 μm in 2010, 2015, and 2020, respectively.<sup>1</sup> Solder has limitations in many areas, including the formation of brittle copper-tin intermetallics that can compromise thermomechanical reliability. Solder also has low electromigration resistance, which is becoming more important as the diameter of interconnects shrinks and current density increases. Flip-chip solder connections are limited to an aspect ratio of roughly unity (1:1 height:diameter), making high aspect ratio (large chip-to-substrate stand-off distance) difficult to fabricate. This causes difficulties with flow in the underfill process. Fragile on-chip interlayer dielectrics require lower stress I/O so as not to cause fracture. Mechanically compliant I/O can be achieved by increasing the aspect ratio of the chip-to-substrate I/O.

An all-copper chip-to-substrate interconnect may eliminate many of the problems with solder. Copper has superior electrical properties compared to solder with respect to both electrical conductivity and electromigration resistance. It also has superior mechanical properties, such as yield stress and Young's modulus, which could allow for the design of mechanically compliant interconnect structures. Having no tin-based materials present eliminates the formation of brittle intermetallics, leading to an improvement in the thermomechanical reliability of the device. Finally, copper interconnects are capable of forming high aspect ratio because they are not melt-cast (do not have to be spherical in shape). This paves the way for fine pitch interconnects with higher stand-off distances and complex shapes, such as shielded coaxial structures, which can support high-frequency I/O.

Previous methods for copper-copper "fusion" connections have been disclosed but are not adequate for replacing solder I/O. In order to obtain adequate bonding between two existing copper surfaces, like copper-wafer bonding, high-temperature annealing (350–450°C) of cleaned copper surfaces under relatively high pressure is required.<sup>2,3</sup> However, this temperature range is too high for organic boards or substrates. An upper temperature limit of ~250°C is required for epoxy (FR-4) or bismaleimide triazine (BT) boards to

avoid degradation. If the copper-wafer fusion processes were used for I/O, there would have to be excellent alignment between the two pillars. The copper-to-copper fusion processes do not allow the two parts to readjust like the molten solder does. Finally, direct copper-to-copper wafer bonding requires either extremely flat surfaces or surfaces that can withstand high pressure to make them flat during bonding, because there is no mechanism to account for vertical (through-plane) height variations. Silicon integrated circuits and organic substrates are not usually flat. Molten solder can be easily expanded or compressed to account for nonplanarity.

In previous work, surface-activated bonding (SAB) has been shown to provide a route for room-temperature copper-copper bonding. The reported bond strength exceeds 6.47 MPa.<sup>4</sup> Room-temperature copper-copper bonding was achieved by bringing together two extremely flat and clean copper surfaces in an ultrahigh-vacuum environment.<sup>4</sup> It also has no tolerance for in-plane misalignment or height variations. Solder, on the other hand, can be easily distorted during reflow to elongate or flatten as needed.

A practical interconnect structure currently used has a reflowable solder cap on the copper pillar.<sup>5</sup> Wang et al. used high-aspect-ratio copper pillars to improve the I/O density.<sup>5</sup> The solder cap avoids the high-temperature copper-to-copper bonding problem. However, the electrical and mechanical limitations of solder still exist.

We recently reported a new approach for making all-copper chip-to-substrate interconnects via electroless plating with low-temperature annealing.<sup>6</sup> Utilizing this method, copper interconnects were fabricated at temperatures safe for organic substrate materials, as low as 250°C. The process allows for the fabrication of high-aspect-ratio structures that can enhance thermomechanical reliability.

In this study, the all-copper system is shown to satisfy requirements for integrated circuit assembly: organic substrate compatibility, thermomechanical reliability, and electrical performance. This paper contains the evaluation of the fabrication and process capabilities of the all-copper interconnect system. The ability to bond copper structures at temperatures compatible with organic substrates is demonstrated, and the process is characterized to find conditions for high bond strength while minimizing the temperature excursion. The dexterity of the process with respect to misalignment between chip and substrate is also evaluated and shown to exceed the capabilities of solder. To implement the all-copper interconnect system, a study has been done to evaluate the design parameters based on thermomechanical compliance and electrical parasitics. The detailed study evaluating these aspects is contained in Part II of this study.<sup>7</sup> The available design space for the copper-pillar system is presented based on the thermomechanical and electrical requirements chosen.

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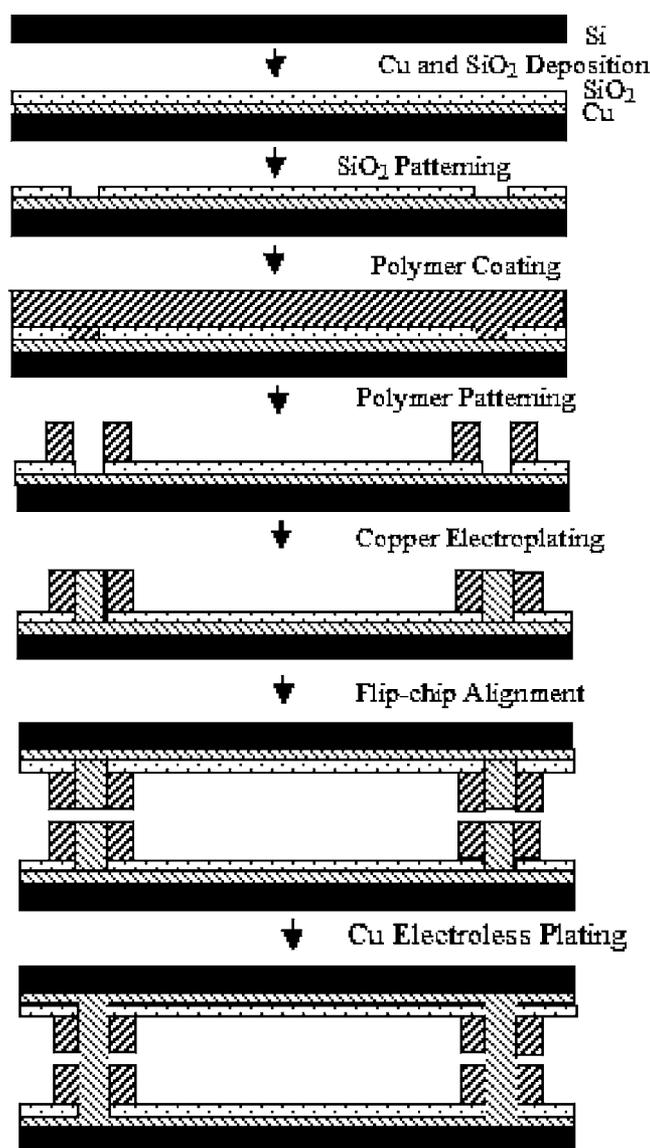


Figure 1. Fabrication process flow diagram.

### Experimental

The fabrication process flow diagram is shown in Fig. 1. A seed layer consisting of Cr/Cu/Ti (50/500/10 nm) was dc sputtered onto a bare (100)4 in. Si wafer. Then, a Unaxis plasma-enhanced chemical vapor deposition system was used to deposit 1.5  $\mu\text{m}$  of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (ShIPLEY Corporation) was spun onto the silicon dioxide surface. After photopatterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO<sub>2</sub> and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 rpm for 60 s. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 min. The Avatrel layer was then photopatterned using 250 mJ/cm<sup>2</sup> dose at 365 nm wavelength. Following exposure, a postexposure bake was applied in an oven at 100°C for 20 min. Then, the layer was developed in BioAct EC-7R Defluxer for 30 s immersed in an ultrasonic bath. The polymer pattern generated high-aspect-ratio hollow-core molds for copper-pillar electroplating.

After the patterning steps, copper pillars were electroplated to fill

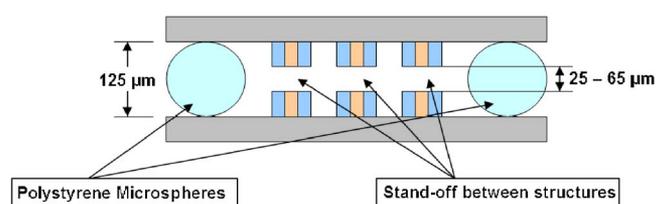


Figure 2. (Color online) Illustration of setting stand-off distance with polystyrene microspheres.

the polymer molds. The electroplating solution contained 30 g/L CuSO<sub>4</sub>, 52 g/L H<sub>2</sub>SO<sub>4</sub>, 40 ppm Cl<sup>-</sup>, 0.5 vol % brightener agent, and 0.5 vol % carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm<sup>2</sup> for 20 h using a phosphorus-doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M-10A flip-chip bonder. Aligned samples were then temporarily held together with a low-temperature melting wax.

The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde, the complexing agent is ethylenediaminetetraacetic acid, and it contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 h with stirring and nitrogen purging. After electroless plating, the samples were annealed in a nitrogen environment for 1 h at various temperatures. In addition, some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and postbonding anneal steps.

To evaluate the effect of height mismatch, polystyrene microspheres (Polysciences Megabeads) with a diameter of 125 ± 2.3  $\mu\text{m}$  were dispersed from a deionized water solution with 1 wt % solids onto the sample surface. These microspheres served to set a known stand-off distance between the sample surfaces illustrated in Fig. 2. To create different separation distances between the pillar top surfaces, pillars of different heights were electroplated onto the samples of 30, 40, and 50  $\mu\text{m}$ , leading to separation distances between the pillar surfaces of approximately 65, 45, and 25  $\mu\text{m}$ , respectively.

After annealing, samples were shear-force tested by fixing the base of one chip and applying a shear load to the other using an Instron 5842. These results were then converted to shear stress using a total surface area average of interconnects placed under load.

To fabricate test samples on the printed circuit-board materials, an alternate approach was taken, as shown in Fig. 3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50  $\mu\text{m}$  thickness. This layer was photodefined to create openings for pillars. BOE was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10 × 10 mm test samples for bonding to fabricated silicon test chips.

### Results

The critical technological and scientific advance of this work is the copper-to-copper joint generated by the electroless plating followed by low-temperature annealing. Minimizing the temperature excursion necessary to create adequate bond strength is necessary for processing with minimal effect on the integrity of the organic substrate materials and other temperature-sensitive components. In order to assess the effects of the anneal temperature on bond strength, samples were annealed for a range of temperatures from 180 to 400°C. The purpose of the 400°C anneal was to decompose the Avatrel polymer molds for direct observation of the all-copper

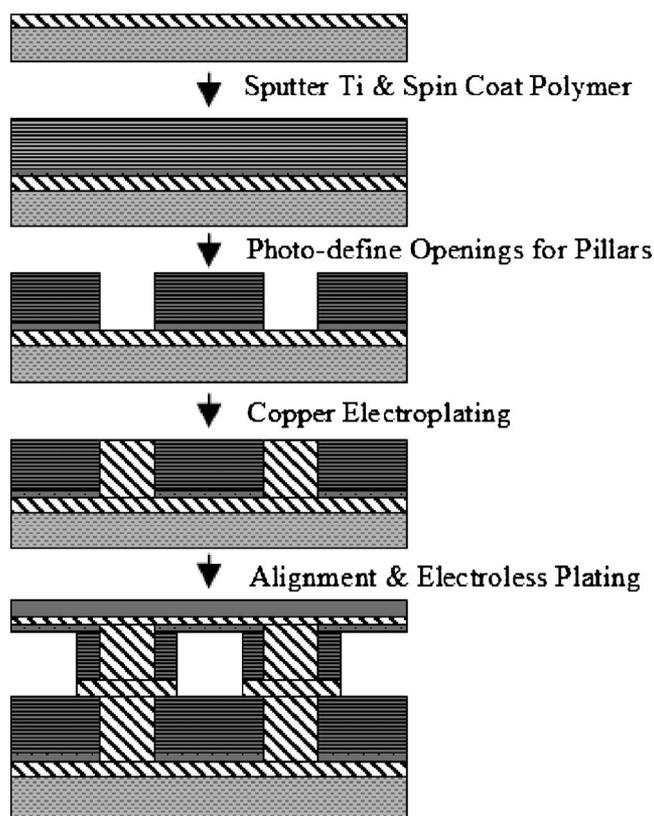


Figure 3. Substrate side fabrication flow diagram.

bonded system. The results of these tests are summarized in Table I. The surface-averaged shear stress required to shear the samples annealed at 200 and 250°C follows a general trend of increasing shear stress with increasing anneal temperature. However, the results at 400°C deviate from this trend due to the absence of the polymer mold (supporting the pillars) when annealed at this temperature, thereby reducing the ability of the system to dissipate stress.

For all tests conducted between 200 and 400°C, the point of failure was at the pillar-to-surface interface and not in the electrolessly plated pillar-to-pillar joint. This shows that the reported stress in Table I is actually measuring the improvement in adhesion of the pillar to the surface with anneal temperature. To confirm this improvement in copper adhesion, an additional anneal step (250°C for 1 h) was added prior to flip-chip alignment and electroless plating.

Table I. Effects of anneal temperature on shear strength for the all-copper system.

Anneal temperature <sup>a</sup> (°C)	Maximum shear stress <sup>b</sup> (MPa)
400 <sup>c</sup>	148
250	189
220	132
200	119
180 <sup>d</sup>	165
150	<20
25	<20

<sup>a</sup> All annealing performed for 1 h.

<sup>b</sup> Based on pillar area and number of pillars.

<sup>c</sup> Avarel is completely decomposed.

<sup>d</sup> Annealed prior to bonding at 250°C to 1 h.

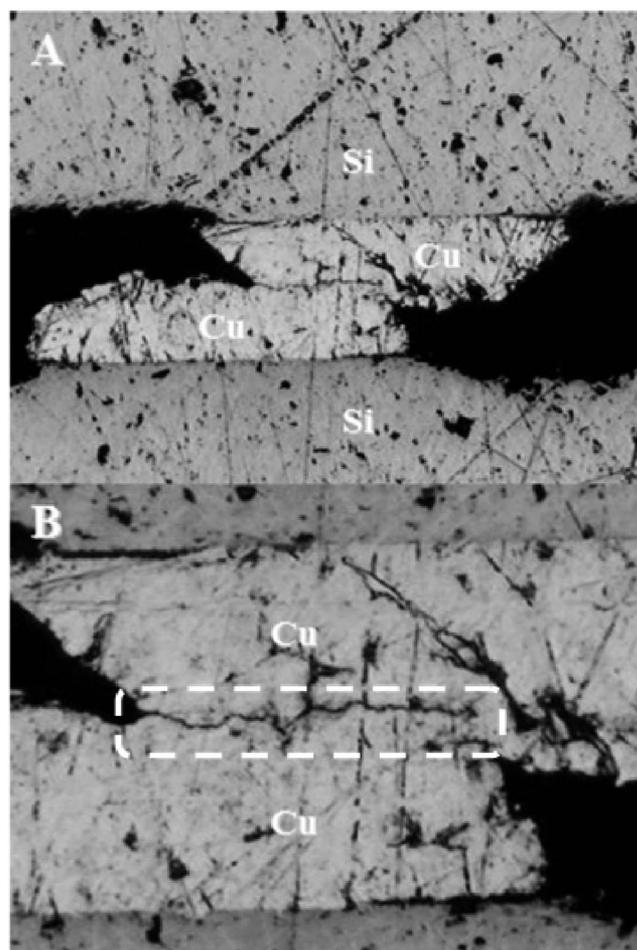
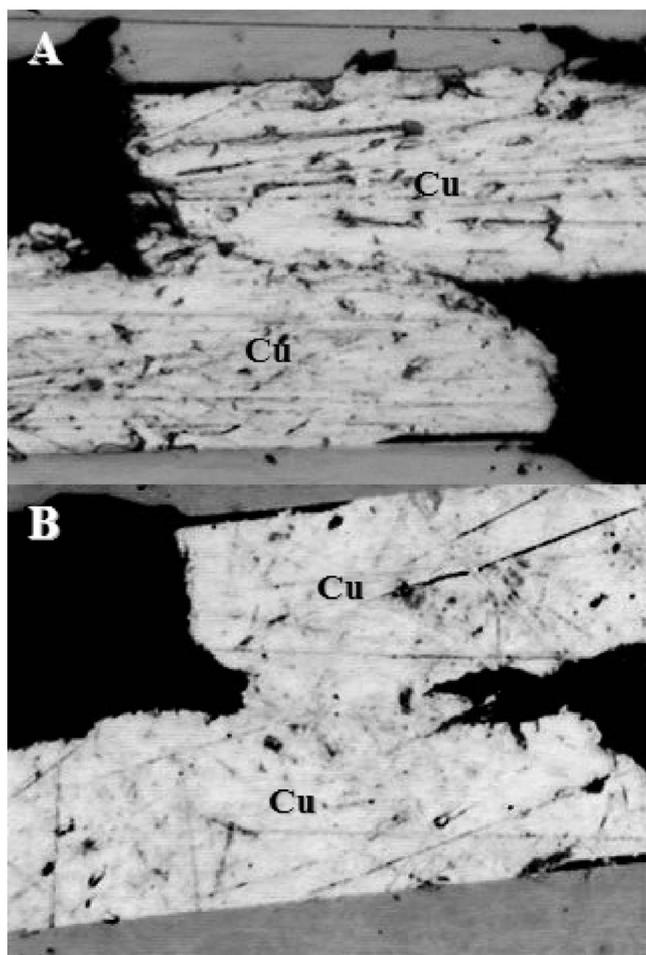


Figure 4. Cross section of bonded copper pillars prior to annealing: (A) full view and (B) higher magnification of bonding interface.

This additional annealing step enhanced the pillar-to-surface adhesion while having no direct impact on the pillar-to-pillar bond.

For the sample annealed at 180°C, the point of failure was the pillar-to-pillar electrolessly plated interface. This shows that the shear stress for the electrolessly plated joint annealed at 180°C was approximately 165 MPa. A bond yield strength of 165 MPa is consistent with the previous results using a single 250°C anneal step after the bonding process. The measured pillar-to-surface adhesion was greater, approximately 189 MPa. A shear stress of 165 MPa is about 75% of the yield stress of bulk electrodeposited copper, 225 MPa.<sup>8</sup> Additional samples annealed at 150°C for 1 h did not withstand the mounting process and were not measured. The unannealed samples (plated but not annealed) also failed during mounting and were not measured.

In addition to testing the mechanical properties of the annealed copper-to-copper pillars, it is also important to characterize the microstructure at the pillar-to-pillar bonding interface. To understand the morphological changes taking place during annealing, cross sections were made of structures prior to and after the annealing process. Figure 4 is a cross section of the two joined pillars after the plating process but before annealing. In Fig. 4 the two pillars are labeled as Cu, and each silicon test surface is labeled. There is a distinct interface or seam between the two electrolessly plated pillars. The interface between the pillars is seen as a dark crevice between the two copper regions. There is little adhesion or bonding between the two pillars at this point, as evidenced by the poor shear test results. Handling of the parts to mount for shear testing was sufficient to break any bonding present.

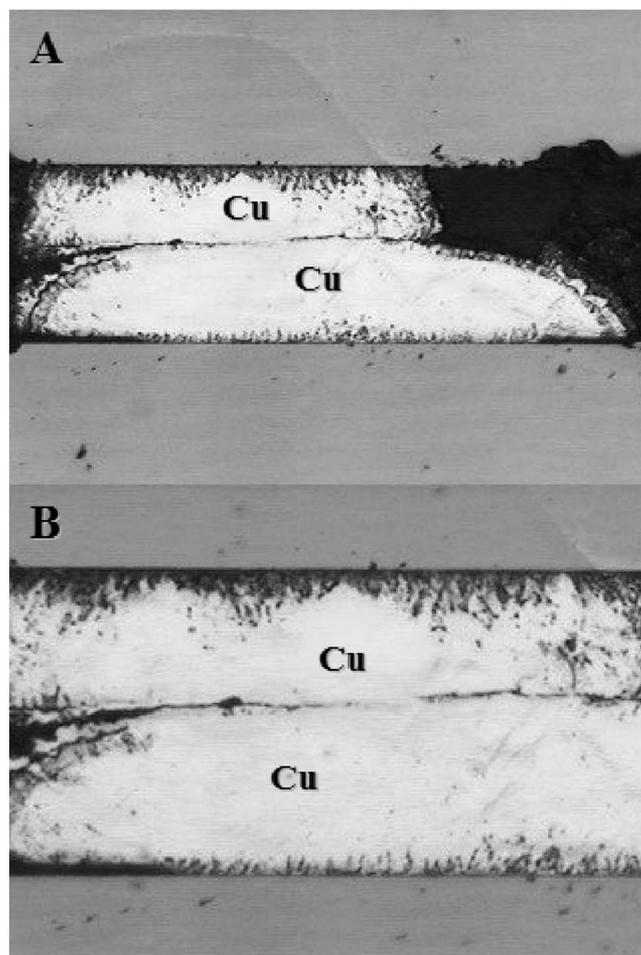


**Figure 5.** Cross section after annealing at (A) 150°C for 30 min and (B) 180°C for an additional 30 min.

Cross sections were made after the 150°C anneal to examine the change in the unannealed interface. Figure 5A shows the interface after a 30 min anneal at 150°C. The interface is still present between the two pillars. After an additional 30 min at 180°C (Fig. 5B), copper-to-copper bonding has occurred and the seam at the interface is not seen. The cross section for a sample annealed at 150°C for 2 h is shown in Fig. 6. The interface can be seen in all the samples bonded at this temperature and time. This shows that even using a significantly longer anneal time, copper-copper bonding does not occur at 150°C. However, all samples annealed at 180°C or greater showed no visible interface and successful bonding. These experiments demonstrate that the minimum temperature for bonding these surfaces is in the range of 180°C.

The ability to compensate for in-plane and through-plane misalignment is important. Solder exhibits excellent ability to compensate for misalignment between contacts during the reflow process. To test the planar tolerance, copper pillars were intentionally misaligned and then taken through the electroless plating and annealing process. Figure 7 shows two pillars that were successfully bonded despite lateral misalignment greater than the diameter of the pillars themselves. Under this severe misalignment, solder would not bond because the molten liquids would not touch each other. The bonded pair of pillars in Fig. 7 survived destructive shear testing, showing that the pillar-to-pillar bond was still stronger than the pillar-to-surface adhesion despite its significantly reduced cross-sectional area and nonuniform geometry.

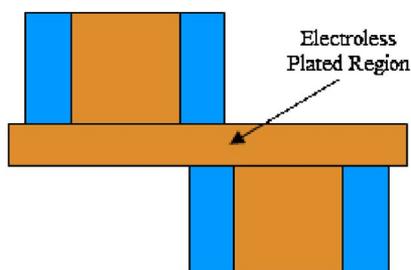
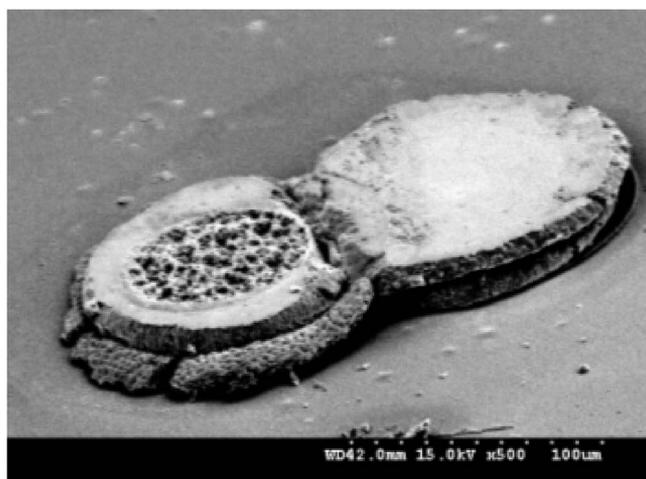
The solder reflow process is able to compensate for nonplanar organic substrates by either elongating or flattening as necessary.



**Figure 6.** Cross section after annealing at 150°C for 2 h: (A) full view and (B) higher magnification of bonding interface.

The ability of the copper-to-copper electroless process to compensate for z-axis height mismatch was assessed. Figure 8 shows scanning electron microscopy (SEM) images of the results of plating samples with separation distances of 25, 45, and 65  $\mu\text{m}$ . The time each sample was in the electroless plating bath was held constant at 24 h. It can be seen in Fig. 8 that the smallest separation distance led to significant outward plating of the copper beyond the diameter of the pillars. For the intermediate separation distance, the joint appears uniform and minimal plating beyond the diameter of the pillars is observed. Finally, at the largest separation distance, the plated joint was entirely contained within the diameter of the structures bonded. It is surprising that the largest separation led to an interior plated joint. It was expected that the plating rate would be less in the center due to the transport difficulties in the system and consumption of reactants. However, this type of plated joint was observed for large areas on multiple samples. The plating rate was fastest in the center, which is where the bonding occurred. An example of an array of bonded structures is shown in Fig. 9. From the results of this test it is evident that the copper-copper plating process can compensate for z-axis separation over a wide range. All three stand-off distances survived destructive shear testing.

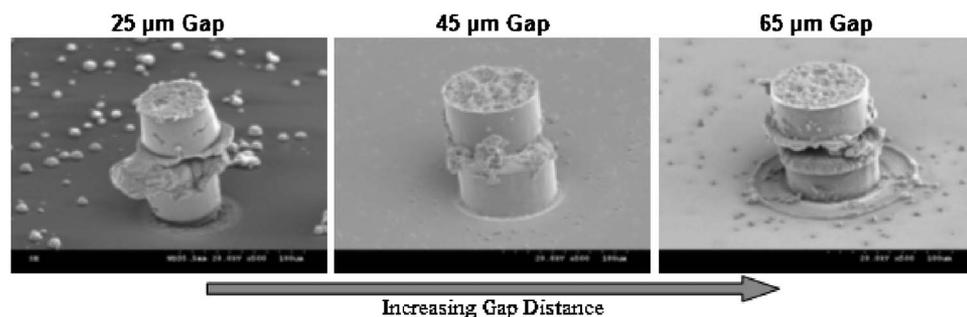
This electroless process is intended to bond silicon chips to organic substrate packages. To demonstrate this, samples were prepared with copper pillars on FR-4 organic substrates and on silicon test chips. Samples were made using flip-chip alignment, electroless plating, and the 180°C (1 h) annealing process described above. Bonding between silicon and an organic board is different from the silicon-to-silicon bonding, because the coefficient of thermal expansion



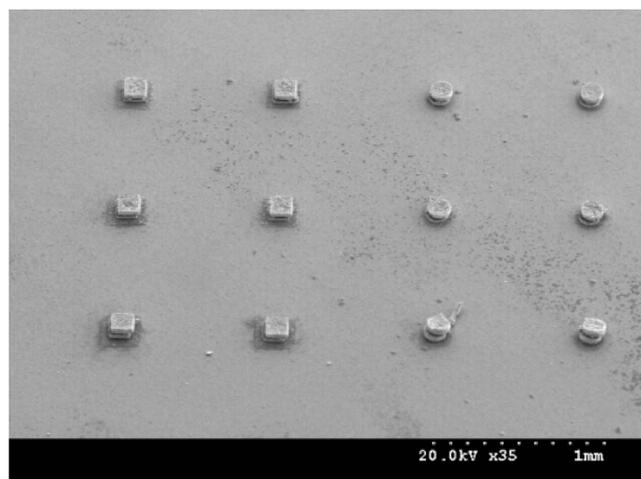
**Figure 7.** (Color online) (above) SEM image and (below) concept of planar misalignment greater than pillar diameter.

sion (CTE) of the organic is higher than silicon. The CTE of silicon is 3 ppm/°C vs 14 ppm/°C for FR-4 and 15 ppm/°C for BT substrates. During the annealing process, the copper interconnects are under shear stress conditions. Brongersma et al. have shown that copper films under stress during recrystallization can exhibit unusually large grain growth, termed super secondary grain growth.<sup>9</sup> Shear loading conditions could potentially be helpful in the bonding process and encourage grain growth in the bonded region. After annealing, the samples were shear tested and compared to silicon-to-silicon bonded samples annealed at the same temperature.

The silicon-to-board bonded samples exhibited different failure characteristics compared to silicon-to-silicon bonding. Because the Avatrel covers the full surface and is not just a polymer collar surrounding the copper pillar on the organic substrate, it cannot detach from the surface as easily during shear-force testing. Therefore, the stress failure takes place in a two-step process. First, the copper pillar is broken from the copper laminate surface (pillar-to-surface adhesion). Then, the pillar is pulled out from the polymer film and remains attached to the pillar on the silicon sample surface. An example of successful bonding chip-to-substrate that survived the destructive shear-force testing is shown in the cross section in Fig.



**Figure 8.** SEM images showing the effects of increasing separation distance between pillar surfaces at distances of (left) 25, (middle) 45, and (right) 65  $\mu\text{m}$ .

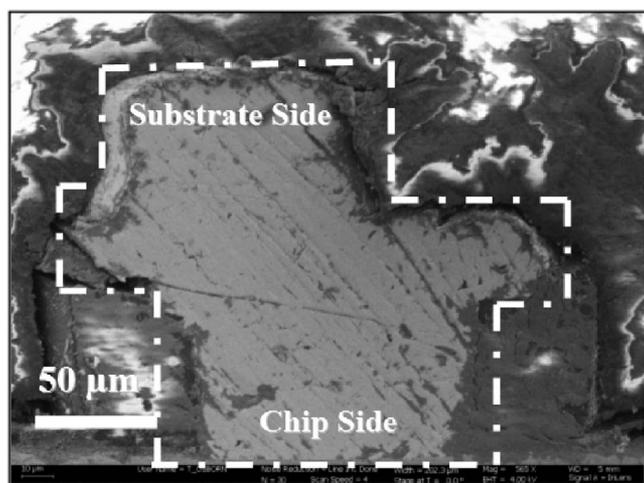


**Figure 9.** SEM image showing bonded and shear-tested structures at the largest separation distance.

10. It exhibits uniform cross section and no interface between the bonded pillar structures. All of the samples tested showed no visible degradation of the organic board materials.

### Discussion

During the electroless plating process, the two copper pillar surfaces grow closer due to the deposition of copper from the electroless bath. As they grow nearer, the surfaces begin to conform to one another and terminate plating near one another ( $\sim 1 \mu\text{m}$ ), as shown in Fig. 4. Constant renewal of the copper surfaces during the electroless plating process maintains clean conditions free of oxides and other contaminants. The seam between the surfaces can then be easily rearranged to form a dense copper-to-copper bond without the application of high temperature or pressure. Unlike copper-copper wafer bonding,<sup>3</sup> the required temperature to drive the bonding process is greatly reduced due to the copper surfaces being free of contaminants and oxide. In addition, the conformal nature of the electroless plated surfaces to one another provides intimate contact without externally applied pressure. Larger voids in the interface can remain and are minimized using the techniques described above. Previously, SAB demonstrated that atomically clean copper surfaces readily bond together at room temperature under modest applied pressure.<sup>4</sup> This result implies that atomically clean copper readily bonds without an elevated-temperature driving force. The necessary temperature for seamless bonding in the all-copper system ( $\sim 180^\circ\text{C}$ ) suggests that the surfaces terminated during the electroless plating process are more readily available to bond than those found in copper-copper wafer bonding<sup>3</sup> but less so than those in SAB.<sup>4</sup> Therefore, while the surface of the two electrolessly plated regions does have some of the clean and readily bondable character found in SAB, there is still a minimum thermal driving force required. The temperature requirement of  $\sim 180^\circ\text{C}$  is in the range



**Figure 10.** SEM cross section of pillars bonded between Si and FR-4.

typical of many metals for recrystallization and grain growth.<sup>10</sup> The surface chemistry mechanism for this unique, low-temperature bonding process will be investigated further in a future manuscript.

Previously, Nakahara et al. and Graebner et al. showed that low-temperature annealing (100–200°C for 24 h) of electroless copper films improved the ductility of the film.<sup>11,12</sup> The change in mechanical properties was shown to result from the removal of molecular hydrogen entrapped in the film and recrystallization and grain growth.<sup>11</sup> The results shown here agree with this improvement in ductility due to low-temperature annealing. The recovery of the ductile nature of copper in the electroless bonded region is important for creating reliable, compliant chip-to-substrate interconnects. However, unlike previous studies, this system is unique in that two distinct electrolessly deposited copper regions are merged during the annealing process. Therefore, the improvement in the mechanical compliance of the all-copper interconnects during annealing comes from three parts, (i) the mixing of the two region interface, (ii) the removal of entrapped hydrogen, and (iii) recrystallization and grain growth. Therefore, the time and temperature requirements for annealing are based on all three processes occurring.

### Conclusions

The three components during low-temperature annealing that drive the improvement in the microstructure and mechanical prop-

erties of the copper–copper bond are (i) elimination of the bonding interface, (ii) hydrogen removal, and (iii) recrystallization and grain growth. Annealing at 180°C removed the interface and yielded bond strength of 165 MPa, which is 75% of the yield stress of electroplated copper. The plating-terminated interface was removed with anneal temperature of 180°C or greater but remained with annealing at 150°C, even with longer anneal times. This showed that there was a minimum temperature barrier to creating a seamless copper–copper bond. The all-copper chip-to-substrate bonding process exhibited superior capabilities compared to solder with respect to both aspects of misalignment (planar and height mismatch). With this process, bonding between silicon test chips and organic substrates has been performed and has demonstrated continuous copper connections without any observable degradation of the organic substrate.

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