Photoelectrochemical etching of semiconductors

by P. A. Kohl

Photoelectrochemical (PEC) etching of III–V semiconductors has been used to fabricate unique structures in electronic and photonic devices, such as integral lenses on light-emitting diodes, gratings on laser structures, and through-wafer via connections in field-effect transistors. The advantages and characteristics of PEC etching are reviewed, and the extension of this processing technique to silicon is addressed. Three-dimensional structures are of great interest in silicon for electronic and micromechanical devices. Silicon is a challenging material to PEC-etch because the oxides formed during etching inhibit the dissolution rate and decrease the spatial resolution. In addition, the long carrier lifetime permits holes to react at unilluminated sites. Nonaqueous solvents provide a processing environment where oxides do not interfere with the spatial resolution and free fluoride is no longer needed in the dissolution of silicon.

Introduction

The electrochemistry of semiconductors has played an important role in the development of integrated circuit (IC) technology. Many of the processes used in IC manufacturing are based on electrochemical principles, and electrochemistry is the foundation for understanding the basic mechanisms of etching, deposition, and corrosion.

One area that is of particular interest is the photoelectrochemical (PEC) etching of semiconductors. PEC etching is a topic encompassing light-induced electrochemical reactions of semiconductors in contact with liquids. The light-induced creation of minority carriers in semiconductors can stimulate spatially-selective or materials-selective etching and deposition reactions.

Much of the PEC etching to date has been focused on III–V semiconductors because of the need for optical components in III–V-based lightwave systems and the ease of PEC processing due to the solubility of the reaction products (e.g., oxides). There is currently considerable interest in PEC etching of silicon for microelectromechanical systems (MEMS) and three-dimensional features for silicon ICs (e.g., trench capacitors).

In this paper, a summary of PEC processing is first presented, followed by new results for the PEC etching of silicon. Although PEC etching may provide a valuable route to fabricating unique structures in silicon, many challenges remain. While the stability of silicon dioxide is an asset in many devices (as compared to compound semiconductors), it makes the PEC etching of silicon very complicated. The use of nonaqueous solvents is one approach to overcoming the formation of oxides during etching.

Basic principles

The semiconductor–electrolyte interface has been discussed in detail [1–6]. In PEC processing, the semiconductor is immersed in a conductive electrolyte, and electrical contact is made to the semiconductor. The semiconductor is biased with respect to a counter electrode, and the potential is measured versus a reference electrode. When the Fermi level of the semiconductor at the semiconductor–electrolyte interface is within the band gap, the density of carriers in the

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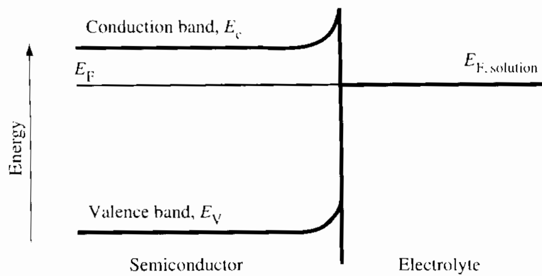


Energy-band structure of an n-type semiconductor in contact with an electrolyte.

semiconductor is usually less than the density of carriers (ions) in the electrolyte, so that a majority of the potential difference across the interface occurs within the semiconductor. **Figure 1** shows the case of an n-type semiconductor in contact with an electrolyte. The charge density in the semiconductor space-charge layer is qN_D, where N_D is the donor concentration. Therefore,

$$\nabla E = \frac{qN_D}{\varepsilon}, \tag{1}$$

where ε is the dielectric permittivity of the semiconductor, E is the electric field, and q is the magnitude of the electronic charge. The width of the space-charge region, w, is related to the potential drop, Φ:

$$w = \sqrt{\frac{2\varepsilon\Phi}{qN_D}}. \tag{2}$$

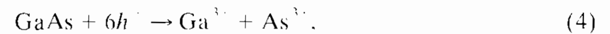
Electron–hole pairs can be photogenerated by irradiating the semiconductor with light whose energy is greater than the band gap. The electrons and holes created within the space-charge region are transported by 1) migration under the influence of the electric field and 2) diffusion due to the gradient in the carrier concentration. The hole concentration, p, is determined from the transport relation for the hole-current density, J_p:

$$J_p = q\mu_p pE - qD_p\nabla p, \tag{3}$$

where D_p is the hole diffusion constant and μ_p is the hole mobility. Photogenerated holes (minority carriers in n-type semiconductors) which reach the semiconductor–electrolyte interface can react with solution species. Electron transfer across the semiconductor–solution interface occurs isoenergetically. Thus, the energy gap and electric field act as a kinetic barrier for electrons (majority carriers in n-type semiconductors) to reach the semiconductor–solution interface. The system is analogous to a semiconductor–metal photodiode, except that ionic conduction replaces the electronic conduction in the metal.

In PEC etching, the potential of the semiconductor is controlled by a power supply or by an oxidizing agent in the case of an electroless process. Three main types of reactions can occur at the semiconductor interface:

1. Oxidation reactions can be induced by holes (h^+) in the valence band. In PEC etching, the presence of a hole in the semiconductor at the electrolyte interface is like a broken chemical bond allowing the ionic dissolution of the semiconductor. For example, with GaAs,



$$GaAs + 6h^+ \rightarrow Ga^{3+} + As^{3+}, \tag{4}$$

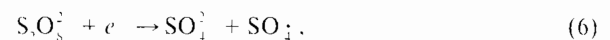
where the particular chemical form of the Ga^{3+} and As^{3+} depends upon the composition (particularly pH) of the electrolyte. For etching to be sustained, the oxidized products must form solvated species.

2. Electrons in the conduction band can initiate the reduction of the semiconductor. For example,

$$GaAs + 3e^- \rightarrow Ga^0 + As^{3-}. \tag{5}$$

This reaction by itself does not lead to etching, because Ga^0 is not a soluble product; however, one can oxidize the Ga^0 in a second step or through an electrochemical process [7] or a chemical process [8].

3. Reduction reactions can be carried out by electrons in the valence band, creating a hole. A strong oxidant is required to carry out this process. Such processes are usually thought of as chemical etchants and not of interest in PEC etching. However, in PEC etching, strongly oxidizing reaction intermediates can be created so that one can locally generate oxidants at the electrode surface [2, 3]. For example, $S_2O_8^{2-}$ ions can be electrochemically reduced via conduction-band electrons, creating SO_4^{-} radical ions. The SO_4^{-} radical ion is a very strong oxidizing agent and can extract an electron from the valence band of the semiconductor, generating a hole:



$$S_2O_8^{2-} + e^- \rightarrow SO_4^{2-} + SO_4^{-}, \tag{6}$$

$$SO_4^{-} \rightarrow SO_4^{2-} + h^+. \tag{7}$$

The hole generated in the valence band can then participate in the oxidation of the semiconductor. In a similar way, quinone can be reduced, creating semiquinone, which can extract a valence-band electron, producing hydroquinone.

In addition to the transport of minority carriers within the semiconductor to the electrolyte interface, the chemical reactivity and dissolution of the reaction products have a strong influence on the rate and spatial

resolution of PEC etching. The chemical reaction for the oxidation–dissolution of the semiconductor, such as that shown in Equation (4) for GaAs, is actually the sum of many, sequential one-electron transfer steps and chemical reactions. However, because of the complexity of the reactions, the sequence of chemical and electrochemical reactions is often treated as a pseudo-first-order reaction in which the rate is directly proportional to $Kp(x = 0)$, where K is the pseudo-first-order rate constant and $p(x = 0)$ is the hole concentration at the semiconductor–solution interface [9]. The rate constant for GaAs has been evaluated in several electrolytes [9].

In summary, the PEC etching of semiconductors is a chemical process initiated by the photogeneration of minority carriers within the semiconductor. The carriers are transported to the semiconductor–solution interface, where a wide variety of chemical processes can be carried out.

Properties of PEC etching

The following useful properties of PEC etching can be understood from the above brief description:

1. *Light-intensity dependence* The rate of etching depends on the rate of minority-carrier photogeneration, and, in many cases, a linear relationship exists between the etch rate and the light intensity.
2. *Spatial selectivity* By spatial modulation of the light intensity, or by providing physical masking, one can "anisotropically" etch semiconductors, forming three-dimensional structures. The spatial resolution, which is discussed for specific cases, is dependent on the semiconductor transport and lifetime properties and on the rate of the chemical reactions.
3. *Band-gap selectivity* On structures having materials with different band gaps, the narrower-gap materials can be selectivity-etched by using light with a spectrum that is absorbed by the narrower-gap materials but not the wider ones.
4. *Dopant-type selectivity* Samples can be biased so that n-type materials are etched but not p-type materials. Alternatively, p-type materials can be isotropically etched in preference to n-type materials. In a more complex scheme, p-type materials can be photoetched [7, 8].
5. *Band-position selectivity* Shifts in the conduction or valence bands can sometimes be used to selectively etch a particular composition by choice of the electrical bias.
6. *Etch-rate monitoring* When an electrical connection to the sample is made, the etch rate and amount of material removed can be monitored by measuring the current flow in the external circuit.
7. *Process and mechanistic definition* Photoelectrochemical studies can often be very useful in designing chemical processes or optimizing existing ones, because one can directly measure the rate of the individual reactions which make up complex processes, such as electroless processes.

Experimental procedures

In PEC experiments, the semiconductor sample is immersed in an electrolyte in a cell which contains an optical window to allow it to be illuminated. Electrical contact is made to the semiconductor. A potential is applied between the semiconductor electrode and a counter electrode (e.g., a piece of platinum) immersed in the same electrolyte. The potential of the semiconductor is measured versus a reference electrode, such as a saturated calomel electrode (SCE), as used in these studies. In this way, the current flowing between the semiconductor and the counter electrode can be recorded as a function of the potential versus the reference electrode. In nonaqueous studies, care must be taken in the proper selection of materials to prevent corrosion. Additional details on the materials used in construction of cells and equipment used in scale-up of processes can be found in the literature (for example, [10, 11]).

Surface relief etching

A class of surface machining (etching) which has been particularly useful for electro-optic devices is the formation of relief features. These features are typically produced by irradiating the surface with a spatially varying light intensity. Much of the work has used III–V semiconductors because they constitute the light-generating and light-absorbing components of many fiber optic systems. **Figure 2** shows a holographic grating etched in a GaAs/AlGaAs substrate.

Diffraction gratings can be etched into semiconductors by a direct holographic process [12–26]. The primary goal is to produce gratings that can be used in the fabrication of distributed feedback lasers, distributed Bragg reflector lasers, filters, and guided-wave couplers. These applications require submicrometer grating periods, usually less than 0.5 μm.

Most of the work has been performed on GaAs [12–18, 21–23, 25], with many of the studies using dilute H_2SO_4:H_2O_2:H_2O in a volume ratio of 1:1:25–100. Very short-period gratings (<0.4 μm) can be etched in GaAs: the total etch depth necessary to achieve a modest surface relief height is large for most optical device applications. That is, if the etched grating is to be 0.4 μm in depth, one may have to remove 0.8 to 4.0 μm (or more) of material (see Figure 2). On the other hand, the longer-period gratings (>0.8 μm), which require the removal of less GaAs, have limited use in waveguide applications. Grating formation in InP has also attracted considerable interest

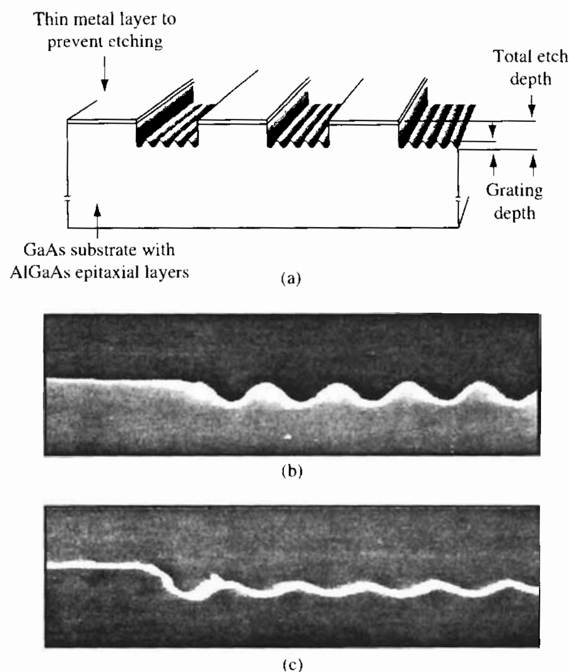


Figure 2

(a) Cross section of a patterned semiconductor for evaluating the spatial resolution of a grating etched into a surface; (b) cross section of a grating etched into a semiconductor with high spatial resolution; (c) cross section of a grating with poor spatial resolution.

because of InP-based optical communications at 1.3- and 1.55-μm wavelengths [19–21, 24, 26].

The analysis of the transport properties of the semiconductor and chemical reactivity of the surface has provided a framework for understanding many of the observations concerning the spatial resolution of PEC etching. A general feature of the experimental results is that the depth etched in the illuminated areas increases more slowly than the depth etched in the unilluminated area as the size of the features becomes smaller. This behavior is due to the diffusion of the photogenerated holes, reducing the spatial contrast of the hole distribution at the interface. Quantitative aspects of this have been discussed in several papers [9, 27–31]. The conclusions are useful in understanding the parameters which control PEC etching and in improving its spatial resolution. The diffusional spreading of the holes is greatly enhanced by a slow chemical reaction. The spatial resolution of gratings can be improved by choosing an electrolyte with a high chemical rate constant, as has been demonstrated in GaAs, AlGaAs, and InP ([30, 31] and references therein). It has been shown that the rate of the chemical reaction can be increased by raising the temperature of the electrolyte [32]. A 25°C increase in the temperature of the electrolyte improved the grating amplitude by a factor of 1.7.

It was also shown that the spatial resolution degraded with deeper penetration of the light into the semiconductor, experimentally accomplished by changing the wavelength. Increasing the lifetime or mobility of the carriers degrades the spatial resolution of the PEC-etched gratings. In effect, the average time before the hole is consumed in the etching reaction was decreased while keeping the chemical reaction velocity constant. This analysis is particularly important because of the long lifetime of carriers in silicon compared to III–V semiconductors. The gratings etched in $Al_{0.3}Ga_{0.7}As$ are about three times deeper than in GaAs because of the lower hole mobility in $Al_{0.3}Ga_{0.7}As$ [31]. Thus, 0.3-μm gratings with high amplitudes can be fabricated in $Al_{0.3}Ga_{0.7}As$, as shown in Figure 2. These results were used to fabricate a 0.35-μm pixellated grating array on a GaAs waveguide with an AlGaAs cladding layer [33].

Matz demonstrated a two-step process for producing high-aspect-ratio gratings in n-GaAs and n-InP. After a shallow grating was formed along the $[01\bar{1}]$ direction by direct illumination of the crystal with a diffraction pattern, the sample was chemically etched [23, 34]. A triangular grating pattern was formed owing to the slow-etching (111) Ga planes. This orientational dependence of the etch rate has been extended to the fabrication of Echelle-type diffraction gratings. GaAs was cut at an angle off the (100) plane toward the (011) plane and etched [35], yielding structures with the interior angles favored by the etching of the Ga-rich surface. The ability to monitor the total etch depth through the current is particularly important in this case.

In addition to gratings, numerous other shapes have been etched (chemically machined) into III–V structures. Integrated microlenses have been etched into InP light-emitting diodes (LED) by projection patterning [10]. The lenses are used to efficiently couple the light from the LED into an optical fiber. The lenses are 100 μm in width and 10 μm in height. The linear relationship between etch rate and light intensity is especially useful. Projection patterning was also used to form dish-shaped openings in an InGaAs layer used as an ion implantation mask for a novel InP/InGaAsP avalanche photodiode [36, 37]. The gradual shape of the dish-shaped structure avoided edge breakdown at a sharp edge.

A via-hole technology has been demonstrated by Podlesnik et al. using an electroless PEC process [38, 39]. They showed that lasers can be used to produce many shapes, including straight-walled holes. It was demonstrated that fiducial patterns on one side of an

n-InP wafer could be PEC-etched through a 90-μm-thick wafer [11]. The metal mask served the dual purpose of the electrical contact and etching mask. The etching was carried out under potentiostatic control. A long-wavelength annular InGaAs photodiode was fabricated by etching a hole through the back of the device using controlled potential etching. The n-InP was photoetched, and the etching was stopped at the p/n junction by proper biasing of the sample [40]. Khare et al. showed that the dopant-type selectivity of n-GaAs on p-GaAs was 15000:1, and the selectivity for n-GaAs on unintentionally doped GaAs was 30:1 [41].

The micromachining of GaAs and InP was studied at high laser intensities [42]. Vertical walls were achieved at high laser intensities, while a crystallographic taper was found at lower intensities. It was observed that conductive n-type substrates etched rapidly, while semi-insulating substrates exhibited enhanced etching only when a metal mask patterned the substrate, providing a low-resistance contact for electron removal. The directionality is believed to be aided by confinement of the processing beam within the hollow etched structure. A 200-μm high-pass filter has been fabricated using PEC etching through a Si-doped n-GaAs wafer [43]. A series of highly anisotropic waveguides with a (3:1) aspect ratio were formed. The effects of orientation and doping were demonstrated on the etching of deep trenches in GaAs [44]. Grooves were etched using a complexing agent (4,5-dihydroxy-1,3-benzene disulfonic acid) for Ga. The pointed bottoms of the grooves were formed along the $[01\bar{1}]$ direction. The high doping density decreased the undercutting of the mask. The field in highly doped material is large, which reduces the lateral diffusion of carriers.

Khare et al. have demonstrated highly selective band-gap etching of AlGaAs [45]. Material having a high Al concentration was PEC-etched in $HCl:H_2O$ 1:20 by using wavelength selectivity. Relative etch rates of 10000:1 and 1000:1 were found for Al mole fractions of 0.15 and 0.05, respectively.

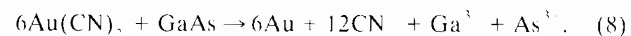
PEC etching has been used to improve the performance of solar cells. Soltz et al. etched antireflection relief microstructures into n-InP [46]: the triangular features were holographically formed parallel to the (011) direction. The improvement in performance of thin-film polycrystalline $CdSe_{0.65}Te_{0.35}$ solar cells was realized by PEC etching and annealing [47]. Maximum quantum efficiencies near 100% were achieved.

A PEC-etching technique was developed for electromechanical sensors, mesa structures, and bipolar and CMOS SiC devices [48–50]. Etch rates as high as 100 μm/min have been achieved: these are the highest reported rates for any room-temperature SiC etching process. High-aspect-ratio structures were formed, and the p/n junction was used as the etch-stop.

The photoetching of n-type semiconductors is relatively straightforward because the photogenerated minority carrier (holes) often leads directly to the decomposition of the lattice. In the case of p-type semiconductors, the etching reaction must depend on the minority carrier (electrons) in order to have photoinitiated process. The ability to PEC-etch p-type materials has been demonstrated with p-InP and p-GaAs. In a two-step process, the p-InP was first photoelectrochemically reduced, forming phosphene and metallic indium [7, 8]. In the second step of the process, the indium was electrochemically oxidized from the surface. In a further development by Quinlan on this same theme, the zero-valent indium was chemically oxidized off the surface using dilute nitric acid [8]. An analogous process for silicon would be very interesting, yielding silane; however, none has been reported.

The observation that mechanical damage inhibited the PEC etching of n-GaAs led Yamamoto and Yano to pattern the surface of a GaAs wafer for selective material removal with the damage induced by ion bombardment [51]. The ion damage provides a recombination center for the photogenerated carriers [52, 53]. The PEC etching was completely suppressed by a 20-keV dose of nitrogen ions at a density of 10^{15} ions/cm^2. The method has been extended by use of a direct-write, focused ion beam (FIB) patterning step. A dose of only 10^{10}–10^{11} ions/cm^2 was needed to write patterns in n-type GaAs, InP, InGaAs, and InGaAsP [53]. The minimum feature size obtained was about 1 μm.

There are several ways in which semiconductor materials can be used to initiate the deposition of metals. The reduction of electroactive solution species (via conduction-band electrons) can be carried out using photogenerated minority carriers in p-type materials or directly on n-type semiconductors in the dark. The filling of small, high-aspect-ratio structures is of particular interest in micromachined devices. The electroless deposition of gold was carried out in GaAs FET via holes by the photoinitiated dissolution of semi-insulating GaAs [11]. The GaAs undergoes photodecomposition, which provides the source of electrons for reducing $Au(CN)_2^-$:

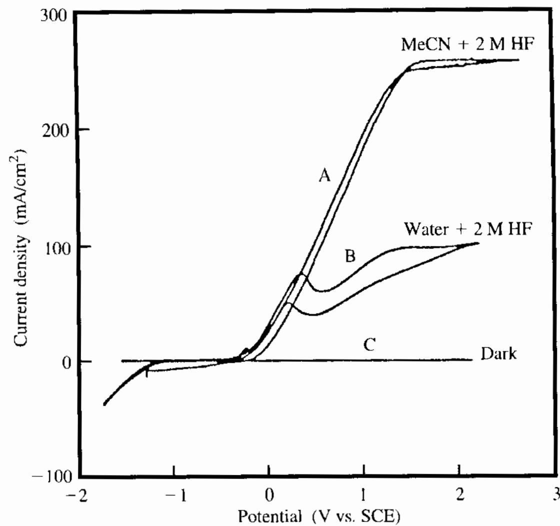


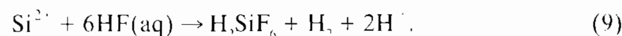
$$6Au(CN)_2^- + GaAs \rightarrow 6Au + 12CN^- + Ga^{3+} + As^{3+}. \quad (8)$$

The Schottky barrier within the GaAs allows only holes to migrate to the semiconductor–solution interface. In this way, the via holes are filled from the bottom to the top.

Silicon etching

The fabrication of three-dimensional structures in silicon (e.g., trench capacitors, sensors, actuators) is of interest in ICs and MEMS devices where silicon is the material of choice because 1) sensors or MEMS devices can be integrated with ICs; 2) the well-established silicon





Current-potential curves for n-Si: Curve A, in 2 M HF in acetonitrile illuminated by a 0.62-mW HeNe laser; Curve B, in 2 M HF in water illuminated by a 0.62-mW HeNe laser; Curve C, in 2 M HF in water in the dark.

processing infrastructure can be used for batch fabrication; and 3) the cost of silicon and silicon-based components is relatively low. The anisotropic chemical etching of silicon relies upon the differential etch rate of the crystal planes of silicon. Since the (111) face etches more slowly, it provides a convenient etch-stop. However, the geometry of the features that can be produced is limited, and because the etching solutions are very corrosive, other materials (e.g., metals and polymers) usually cannot be exposed. Thus, the PEC etching of silicon may provide a high-value processing technique for etching unique features in silicon.

The overall reaction for the anodic dissolution of silicon in aqueous, fluoride-containing media has been discussed previously [54, 55]. The first step is the formation of the doubly oxidized surface intermediate, Si(II). The rate of formation of Si(II) is dependent on the hole concentration at the silicon–solution interface. The Si(II) can react with the aqueous electrolyte, producing hydrogen gas and Si(IV), which can be solvated by fluoride ions:

$$Si^{2+} + 6HF(aq) \rightarrow H_2SiF_6 + H_2 + 2H^+. \tag{9}$$

Under these conditions, porous silicon structures are formed. Alternatively, at higher potentials, the silicon can be oxidized directly to Si(IV), forming a mixed oxide/fluoride where four electrons per silicon and electropolishing are observed. In both cases, the reaction with water and formation of oxides (intermediates or products) limits the velocity of the overall chemical reaction. In spite of the hydrogen evolution problems and the rate-limiting nature of the oxide intermediates, Eddowes found that the 20-μm-deep features could be etched with "quite sharp" spatial resolution [55].

Some of the parameters for achieving higher spatial resolution for PEC etching of silicon in aqueous solvents have been discussed [56–58]. They qualitatively state several of the conclusions which were quantitatively found for III–V semiconductors:

1. Materials should be n-type or semi-insulating.
2. Minority carrier diffusion lengths should be small.
3. The Schottky barrier formed at <1 V should be adequate for PEC etching.
4. Soluble ions should be formed (so that the reaction rate is not slowed by the precipitation of products).
5. A large contrast should be provided between the photoetched and nonphotoetched regions [56].

The investigation of the mechanism of silicon etching has been stimulated by the observation of luminescence from porous silicon. Lehmann and Gosele have described a mechanistic view of the hydride-terminated silicon surface and proposed a route to the formation of molecular hydrogen during oxidation [Equation (9)] [54, 59]. The mechanism loosely accounts for the role of water and surface oxides in the reaction as a competition between water and fluoride for adding across the back-bonds (Si–Si bonds); however, it does not address the role of water in the attack and complexation of the hydride-terminated surface.

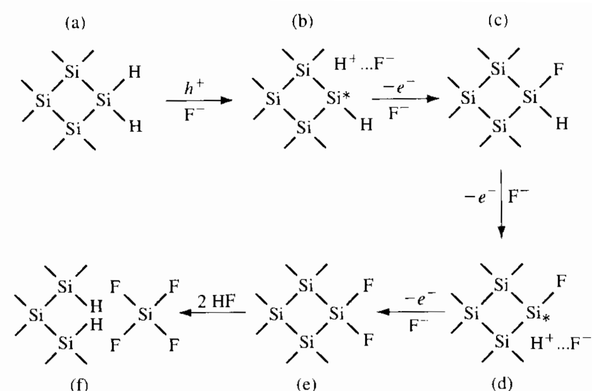
The formation of porous silicon in aqueous solutions occurs at potentials less than the critical current peak, as shown in **Figure 3** for the curve with water + 2 M HF (Curve B). The role of water in the formation of surface oxides was addressed by Propst and Kohl by use of nonaqueous solvents in the PEC etching and dissolution of silicon [60, 61]. Figure 3 shows the photoanodic current for n-Si in 2 M HF in acetonitrile (Curve A) using the same 0.62-mW HeNe laser source as in the water + 2 M HF solution. No critical current peak was observed. The current was much greater in the absence of water (the quantum efficiency is about 3), and the pores were very different in shape. The higher current density is a result of current multiplication, which can occur to a greater extent when water is not present. At low current densities in water, two electrons per photon absorbed are observed in the external circuit (quantum efficiency of 2). At higher currents in water, the quantum efficiency goes to 1. Current multiplication is due to electron injection into the conduction band during oxidation after the photoinitiation step. The dissolution-limited current density was more than 1.4 A/cm² for p-type silicon, which is much larger

than can occur in aqueous solutions, where the current is limited by the formation and dissolution of oxides, and electropolishing takes place.

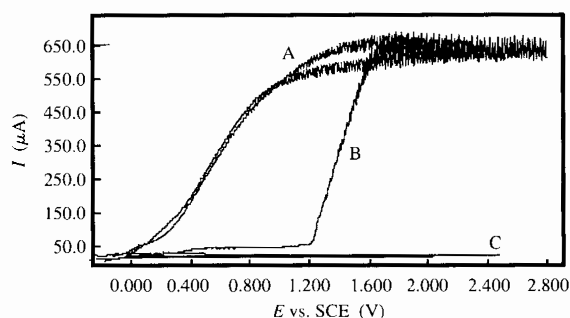
On the basis of the HF–MeCN results, a mechanism for the oxidation–dissolution of silicon in HF containing electrolytes has been proposed; it is shown in **Figure 4**. The initial surface is hydrogen-terminated, as determined by infrared spectroscopy and supported by *ab initio* calculations [62, 63]. The reaction begins with the generation of holes, either thermally generated or photogenerated. The holes drift under the applied bias to the solution interface where they can react [Figure 4(a)]. A radical and a proton are formed as a result of the hole-initiated reaction. The radical can easily be oxidized, thereby injecting an electron into the conduction band. This results in two electrons per photon, or current doubling. The positively charged silicon can now be complexed by a fluoride ion [Figure 4(c)]. Owing to the highly electronegative nature of fluoride, the adjacent silicon–hydrogen bond is destabilized, thereby increasing its reactivity. The destabilized silicon–fluoride bond is then oxidized, forming a radical and a proton. The second radical is easily oxidized [Figure 4(d)], leading to a second fluoride termination of the surface. The fluoride surface destabilizes the silicon back-bonds, allowing HF to be inserted easily across them [Figure 4(f)]. Fluoride adds to the SiF_2 entity producing SiF_4, which dissolves into the electrolyte in the form of silicon hexafluoride and leaves a monohydride-terminated surface.

By means of this mechanism, the role of water can be better understood. If the silicon surface reacts with water instead of the fluoride, the surface becomes terminated by silicon oxides or oxyhydrides. These oxides/oxyhydrides are kinetically slow to dissolve. The silicon hydride adjacent to a silicon oxide/hydroxide is thermodynamically more stable than a silicon hydride adjacent to a Si–F bond, because the fluoride is more electron-withdrawing than the oxide/hydroxide. As a result, the silicon hydride is less reactive (more stable) when the surface is oxide/hydroxide-terminated, and as a result the etch rate is lower. Holes arriving at the silicon–solution interface must wait for the oxide to dissolve in the HF solution, allowing the hole time to diffuse from the point of illumination or to recombine. Thus, spatial resolution is sacrificed. By removing the water, the oxide/oxyhydride formation is avoided and the etching behavior is improved.

The removal of water from the etching solution has a benefit that is potentially even more important. One of the functions of the free fluoride in aqueous solutions is to dissolve silicon dioxide. The dominant species responsible for SiO_2 dissolution in aqueous HF solutions is HF_2^- [64]. Since silicon dioxide formation does not occur in the nonaqueous solutions used here, free fluoride is not needed for oxide dissolution. Fluoride is still needed for



Mechanism for the photo-oxidation of silicon.



Current-potential behavior of n-Si: Curve A, in 2 M HF in acetonitrile illuminated by a 0.62-mW HeNe laser; Curve B, in 0.5 M $TBABF_4$ in acetonitrile illuminated by a 0.62-mW HeNe laser; Curve C, in 2 M HF in acetonitrile in the dark.

complexation of the oxidized silicon (resulting in dissolution as SiF_6^{2-}); however, it can take the form of a less toxic complex. **Figure 5** shows the current-voltage behavior for illuminated n-type silicon in 2 M HF in acetonitrile (Curve A), 0.5 M tetrabutylammonium fluoroborate ($TBABF_4$) in acetonitrile (Curve B), and n-type silicon in the dark in 0.5 M $TBABF_4$/acetonitrile (Curve C). In the HF solution, the flat-band voltage was approximately −0.3 V vs. SCE. As the potential was swept positive of the flat-band potential, the current increased and formed a plateau in the region from 1 V to 3 V vs. SCE. In the $TBABF_4$ solution (Curve B), only a small photocurrent was observed over the range of −0.3 to

1.0 V vs. SCE. At approximately 1.2 V vs. SCE, the photocurrent rose and formed a photocurrent plateau. Replacement of the HF with $TBABF_4$ shifted the potential of the photocurrent plateau to more positive potentials. The photocurrent resulted in the sustained oxidation and dissolution (etching) of the silicon. The oxidized silicon has a high affinity for fluoride ions; it is able to strip a fluoride ion from fluoroborate as a result of this high affinity, in the absence of water. In the presence of water, the oxidized silicon can react with aqueous species, so fluoroborate is not an acceptable complexing agent. Four other fluoride-containing salts were investigated to demonstrate this point: tetrabutylammonium hexafluorophosphate, tetrabutylammonium trifluoromethanesulfonate, sodium hexafluoroantimonate, and potassium hexafluoroarsenate. The water content of the solutions was measured using the Karl Fischer coulometric titration technique, and they were found to contain 50 to 100 ppm of water. N-type silicon could be PEC-etched in each of these solutions, similar to $TBABF_4$.

The elimination of free fluoride has several benefits. The toxicity to humans of the fluoride salts is considerably less than that of HF or other salts that result in a high concentration of free fluoride. Second, silicon oxide is not soluble in solutions containing $TBABF_4$ or the four other salts mentioned above. Thus, it is possible to etch silicon with oxide present, or to use silicon dioxide as an etch mask for PEC etching. This may prove valuable in the formation of three-dimensional features late in the device process sequence, when oxides are present as part of the device.

The origin of the shift in the current plateau for the non-HF electrolyte may be due to the nature of the surface termination during etching. A larger number of positively charged surface states may be formed during the oxidation–dissolution process owing to a lack of nucleophiles, resulting in a "shift" in the flat-band potential to more positive values. Since HF is no longer present to add across the –Si–Si– back-bonds, this step must be different, resulting in a different number of electrons per photon for the overall reaction. Considerable work must still take place to increase understanding of the effects of the solvent on the dissolution process and the effects of the long diffusion length of the holes on the spatial resolution of silicon PEC etching.

Summary

Photoelectrochemical etching of III–V semiconductors has been used to form unique structures in electronic and photonic devices; these include integrated lenses on light-emitting diodes, gratings on laser devices, and through-wafer via connections in field-effect transistors. The PEC etching of silicon is of considerable interest for micromachining devices in silicon wafers, because it offers several advantages over conventional processes. However, two significant obstacles remain for the PEC etching of high-spatial-resolution structures in silicon: the interference of oxides and the long diffusion length of carriers in silicon. Nonaqueous solvents provide a nonoxide processing environment; however, many technological details remain to be addressed.

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