Processing and Performance of Gold MCM's

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Abstract—The use of gold metallization in multichip modules (MCM's) has been investigated for the purpose of achieving simplified processing and high reliability. A process has been developed for producing multilayered, gold metallization thin film MCM (MCM-D) structures which reduces the number of processing steps compared to copper metallization. Multilayered gold—polymer and gold—SiO₂ test devices have been fabricated to evaluate the electrical and mechanical properties of the structures. The adhesion of a variety of dielectrics has been achieved by blanket coverage of the noble metal with a single step adhesion layer. The processing, performance, adhesion layer, and cost of gold MCM-D structures on silicon substrates have been analyzed.

I. INTRODUCTION

Thin film multichip module (MCM-D) technology offers significant weight, volume, and potential cost savings coupled with higher performance for electronic systems. A critical issue in MCM manufacturing and research is achieving high reliability with cost-effective processing. Reliability is a crucial issue since many applications for MCM’s require tremendous heat dissipation, operation from dc to gigahertz frequencies, and high performance functionality over wide extremes of temperature, vibration, shock, humidity, and atmospheric pressure. MCM’s are also needed for high-speed conduction networks in order to successfully complement both conventional CMOS-based digital computing systems operating at 100-MHz clock rates, and advanced silicon ECL and GaAs-based processors operating at hundreds of megahertz or even low gigahertz clock rates [1].

To address these objectives, a process has been developed for producing multilayered, gold metallization MCM-D structures. The inertness of gold offers several immediate advantages. First, because there is no danger of corrosion, gold MCM’s offer the promise of eliminating corrosion induced failure modes which have been a critical factor in the design of certain MCM technologies. Second, the use of gold confers full reign over current dielectric materials, allowing the user to choose the insulator that best meets the application. Third, no corrosion protection layer is required during gold MCM fabrication, nor is a final bond pad layer necessary as soldering directly to the top gold metallization layer is feasible, particularly with indium-based solders. This results in a reduction in the number of processing steps that can have a large impact on both the fabrication costs and the overall process yield. Furthermore, gold metallization provides an excellent vehicle for examining the properties of the insulators, since the lack of metal—insulator chemical interactions allows the dielectric properties to be isolated. However, the adhesion of insulators to gold requires special attention due to the lack of an appropriate oxide.

MCM test structures using organic and inorganic films as the dielectric layers have been fabricated to evaluate the electrical and mechanical properties of the structure. A gold metallization process, comprised of sputtering and electroplating, was used to produce the conduction paths. A low-cost blanket adhesion layer of titanium was used to provide adhesion to all of the insulators investigated. The multilayered structures were produced using sloped vias in the dielectric material to provide interlayer contact. The characterization of the electroplated gold film, the titanium adhesion layer, and the cost benefits of gold MCM’s are described in this paper.

II. EXPERIMENTAL

A. Fabrication

The processing steps for the fabrication of an MCM test structure using gold metallization are shown in Fig. 1. Thermally oxidized, 4-inch diameter silicon wafers were used as the substrates. Each metal layer was formed by sequentially sputtering 75 Å of titanium, 1200 Å of gold, and then another 75 Å of titanium (Fig. 1(a)). The bottom layer of titanium served as an adhesion layer between the gold seed layer and the substrate, while the top titanium layer served as an adhesion layer between the subsequent photoresist and the gold. This top adhesion layer of titanium was completely removed in the course of fabricating the metal layer. The first metal pattern was lithographically patterned using 3-μm thick positive photoresist. The exposed titanium adhesion layer was then chemically etched using a 0.09 M ethylenediamine tetraacetic acid (EDTA)/hydrogen peroxide solution (Fig. 1(b)). This titanium etch is specific to the titanium and does not etch gold, SiO₂, or polymers. The titanium etch rate was 50 Å/min and was used to expose the seed layer of gold for electroplating.

A gold electroplating cell was designed and constructed to simultaneously electroplate three wafers. An additive free, pH 7 potassium gold cyanide (KAu(CN)₂) bath was selected for its purity (absence of additives which can be deleterious to the conductivity) and neutral pH (allowing the use of any insulator without chemical attack). The conductive paths were plated at a current density of 2.5 mA/cm², providing a gold deposition rate of 0.16 μm/min (Fig. 1(c)). Once the first metal layer was electroplated and the photoresist was removed, the seed layer of gold and the titanium adhesion layers were alternately etched away (Fig. 1(d)). At this point in the processing, the top 75-Å titanium adhesion layer has been completely removed.
The gold seed layer was etched using a KI/I\textsubscript{2} solution in an ultrasonic bath to improve the resolution of the plated structures. The etch rate of both the sputtered and plated gold was 1000 Å/min.

The patterned substrate was then sputtered with a 12-Å titanium adhesion layer in preparation for dielectric deposition (Fig. 1(e)). Although titanium was sputtered, the layer quickly oxidized to insulatory TiO\textsubscript{2} (further discussion of the adhesion layer will follow in Section III). The chemical inertness of gold and the versatility of the titanium adhesion film provided a means of constructing metal–insulator structures with a wide variety of dielectrics. Structures using SiO\textsubscript{2}, numerous polyimides, polyquinolines, and benzocyclobutene have all been fabricated with this gold metallization process. In our test structure, the SiO\textsubscript{2} was deposited by plasma enhanced chemical vapor deposition (PECVD) while the organic insulators were spin coated and cured at an appropriate temperature. A complete listing of these materials and selected
TABLE I
DIELECTRIC MATERIALS SUCCESSFULLY INTEGRATED INTO GOLD MCM FABRICATION PROCESS. THE PHYSICAL PROPERTIES WERE OBTAINED FROM THE MANUFACTURERS

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Vendor</th>
<th>Name</th>
<th>Description</th>
<th>Modulus (GPa)</th>
<th>CTE (ppm/°C)</th>
<th>Stress (MPa)</th>
<th>Dielectric Constant</th>
<th>Cure Temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyimide</td>
<td>Amoco</td>
<td>Ultradel 7501</td>
<td>Photodefinable</td>
<td>359</td>
<td>24</td>
<td>35</td>
<td>2.8</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td>DuPont</td>
<td>PI-2545</td>
<td>PMDA-ODA</td>
<td>140</td>
<td>20</td>
<td>35</td>
<td>3.5</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PI-2555</td>
<td>HTDA-ODA</td>
<td>245</td>
<td>40</td>
<td>36</td>
<td>3.3</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PI-2566</td>
<td>Fluorinated</td>
<td>245</td>
<td>38</td>
<td>35</td>
<td>3.0</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PI-2611D</td>
<td>Low Stress</td>
<td>845</td>
<td>3</td>
<td>6</td>
<td>2.9</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td>Hitachi</td>
<td>PIQ-L100</td>
<td>Photodefinable</td>
<td>612</td>
<td>25</td>
<td>36</td>
<td>3.0</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td>National</td>
<td>EL-5512</td>
<td>Fluorinated</td>
<td>281</td>
<td>38</td>
<td>42.9</td>
<td>2.8</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td>Starch</td>
<td>EL-5010</td>
<td>Isoimide</td>
<td>307</td>
<td>34</td>
<td>35.6</td>
<td>3.1</td>
<td>350-400</td>
</tr>
<tr>
<td></td>
<td>OCG</td>
<td>Probimide 293</td>
<td>Preimidized</td>
<td>28</td>
<td></td>
<td>36</td>
<td>3.3</td>
<td>185-250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Probimide 412</td>
<td>Photodefinable</td>
<td>40</td>
<td></td>
<td>36</td>
<td>3.0</td>
<td>350-400</td>
</tr>
<tr>
<td>Benzocyclobutene</td>
<td>DOW</td>
<td>Cyclotene 3022</td>
<td>BCB</td>
<td>239</td>
<td>65</td>
<td>37</td>
<td>2.7</td>
<td>200-250</td>
</tr>
<tr>
<td>Polyquinoline</td>
<td>Allied Signal</td>
<td>PQA 4015</td>
<td>PQA</td>
<td>211</td>
<td>7</td>
<td>5-10</td>
<td>2.8</td>
<td>350</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>PECVD</td>
<td>SiO2</td>
<td>Inorganic</td>
<td>7000</td>
<td>0.5</td>
<td>-100 to -400</td>
<td>4.2</td>
<td>250-400</td>
</tr>
</tbody>
</table>

properties are shown in Table I. After the dielectric deposition, via holes were lithographically patterned and the vias were reactive ion etched (Fig. 1(f)). The etching parameters were chosen such that the vias had sloped walls of at least 10° from the normal to ensure proper step coverage in the next metallization process. The photoresist was then removed in an oxygen plasma. To begin the next metallization process, a second Ti/Au/Ti seed layer was sputtered (Fig. 1(g)). This second metal layer was lithographically patterned and the exposed titanium was removed (Fig. 1(h)). Finally, the signal layer was electroplated, the photoresist stripped, and the extraneous Ti/Au/Ti sputtered layers etched away (Fig. 1(i)). This fabrication cycle was repeated to produce all additional metal–insulator layers.

B. Experimental Methods

The conductivity and density measurements were required to measure the effects of thermal processing on the electrical properties of the gold films. A four-point probe was used for the conductivity measurements to eliminate surface resistivity effects. The thickness of the plated gold, then necessary to calculate the slice resistances, was measured with a surface profilometer. The density of the plated gold films was measured using a helium pycnometer.

The residual stress in the plated gold film was measured to characterize device reliability under adverse operating conditions, primarily thermally induced stresses which can lead to cracking, adhesion loss, or electromigration failures [2]. The residual stress experiments were performed with a Flexus 2320 laser leverage system, and a schematic of the residual stress measurement can be seen in Fig. 2. The residual stress was obtained by measuring the change in the original radius of curvature of a bare silicon wafer created by the deposition of a stressed thin film on the substrate. Similarly, the residual stress of the gold film versus temperature was obtained by measuring the change in the original radius of curvature of a Si/Au composite as it was subjected to several heating cycles.

![Fig 2. Residual stress measurement schematic.](image)

The numerical value for the residual stress, , was calculated by the following expression:

\[
\sigma = \frac{1}{6(1-\nu)} \frac{E}{t} \left( \frac{1}{R_{\text{uncoated}}} - \frac{1}{R_{\text{coated}}} \right)
\]

where \( R_{\text{uncoated}} \) and \( R_{\text{coated}} \) are the radii of curvature of the silicon substrate before and after gold deposition, respectively, \( E \) is Young’s modulus of the substrate, \( \nu \) is the Poisson’s ratio of silicon, and \( t \) is the thickness of the silicon substrate. Typical values for the Young’s modulus and Poisson’s ratio for silicon are 1.9 × 10¹¹ N/m² and 0.27, respectively [3].

III. RESULTS AND DISCUSSION

A. Gold Characterization

The results of the conductivity and density measurements are shown in Table II. The density and the conductivity of unprocessed electroplated gold were each measured to be 90% of the bulk values. To simulate the effects of prolonged, high temperature processing, which is typical for the deposition of multiple dielectric layers, plated gold films on silicon substrates were placed in a 200°C oven for 60 h. This treatment resulted in an additional 10% decrease in the measured conductivity values. This temperature cycle was restricted to
a maximum of 200°C due to potential cracking of full-surface metal films. An identical 10% decrease in conductivity was observed for signal lines after actual polymer processing at temperatures exceeding 350°C, though for much shorter time periods.

The 10% difference in the conductivity between the freshly plated and bulk gold can be attributed to the lower density of the plated gold, which was approximately 10% below the bulk value. Upon thermal processing, the additional 10% loss in conductivity observed can be correlated to foreign molecules that can become incorporated into the gold. These foreign molecules typically originate from the supporting electrolyte in the plating solution during the electroplating, or from the insulators encapsulating the gold during the dielectric processing. When these molecules are dispersed throughout the gold, they have little effect on the electrical properties of the metal. During the high temperature treatment, however, these impurities redistribute themselves to concentrate at the grain boundaries and effect the observed decrease in conductivity.

However, the critical factor to consider is the postfabrication conductivity of the metal. During the repeated high temperature cycle processes necessary for dielectric applications, the conductivity of a gold MCM may fall as low as $3.36 \times 10^4 \text{ (}\Omega \cdot \text{m})^{-1}$. This 20% decrease from the unprocessed value compares with similar copper structures, where the asfabricated conductivity may fall as low as $2 - 3 \times 10^4 \text{ (}\Omega \cdot \text{m})^{-1}$.

The conductivity of copper decreases not only for the same reasons listed previously, but also because some of the barrier metal layer required for corrosion resistance of the copper structures can diffuse into the copper and additionally degrade the electrical properties of the metal. Thus although the bulk conductivity of gold is less than that of copper, there are certain processing situations which can result in similar postfabrication conductivities.

The results for the residual stress experiments are shown in Fig. 3. The residual stress of freshly plated gold was 27 MPa ($27 \times 10^3 \text{ dynes/m}^2$). This room temperature tensile stress resulted from the CTE mismatch between the gold and the silicon substrate as the composite was cooled from the plating temperature of 500°C, an approximately zero stress condition. Then, in order to characterize the stress behavior in the gold films as a function of thermal history, the residual stress was constantly monitored as the temperature was cycled between room temperature and 400°C, with heating and cooling rates of 3°C/min. The residual stress versus temperature curve followed the general behavior seen for films of this type. As the composite was heated during the first cycle, the slope matched the slope expected from the magnitude of the Au/Si CTE mismatch as the gold expanded faster than the silicon substrate. The elastic limit of the composite was reached at approximately 200°C, above which the plastic deformation in the metal film continually mitigated any increases in the compressive stress as the temperature increased. As the composite was cooled, a brief elastic response was then followed by another plastic deformation period as the elastic limit of the composite was once again exceeded by the residual stress in the film.

The second and third heating cycles behaved precisely as the first, except the curve had been pushed permanently to the right by the vacancy consumption, grain growth, and recrystallization that was unique to the first cycle. The final residual stress value of the gold film was 130 MPa. The cooling slopes do not match the slope expected from the Au/Si CTE mismatch, a behavior attributable to the plastic deformation occurring in the film; had the plastic deformation not occurred, the final residual stress value would have been considerably higher.

Flinn, Gardner, and Nix [3] described the ideal stress behavior for aluminum films where the elastic and plastic behaviors nearly form a rectangle during a comparable temperature cycle. Flinn et al. also suggested that the true stress-temperature curves, as in Fig. 3, are rounded at the upper-right and lower-left corners due to a mixture of the two behaviors, elastic and plastic, across the surface of the wafer. The residual stress in Fig. 3 is cyclic for the heating and cooling processes, and the stress in the gold film did not increase above 130 MPa as long as the highest temperature in the thermal history of the film was not exceeded.

Thermally induced stress is a concern in the microelectronics industry both as a failure mechanism and because the resultant voids play a dominant role in subsequent electromigration failure. The final residual stress magnitudes for copper and aluminum films are similar to those for gold [5]. It has been shown, however, that copper lines can show severe stress-induced voiding when encased with certain barrier metal layers, directly leading to increased electromigration failures [2]. Because electromigration is typically absent in gold, such problems associated with residual stress are greatly simplified. Failure mechanisms such as these are among the motivating forces in the search for dielectric materials that can be processed at temperatures below 250°C.
TABLE III
RESISTANCE VALUES OF VARIOUS TITANIUM ADHESION LAYER
THICKNESSES. OXIDATION TEMPERATURE WAS LIMITED TO 95°C IN AIR

<table>
<thead>
<tr>
<th>Length of oxidation in air at 95°C</th>
<th>resistance of 10-Å Ti layer</th>
<th>resistance of 20-Å Ti layer</th>
<th>resistance of 30-Å Ti layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 min</td>
<td>1.70 x 10^8 Ω</td>
<td>1.60 x 10^7 Ω</td>
<td>10 Ω</td>
</tr>
<tr>
<td>5 min</td>
<td>open circuit</td>
<td>1.30 x 10^8 Ω</td>
<td>52 Ω</td>
</tr>
<tr>
<td>10 min</td>
<td>open circuit</td>
<td>open circuit</td>
<td>100 Ω</td>
</tr>
</tbody>
</table>

B. Adhesion Characterization

In applications in which gold is to be used for the conducting layers, an underlayer must be provided to ensure adhesion [6]. Titanium was chosen for investigation as it showed the most promise among the common transition metals due to its high heat of formation of the oxide, indicative of good adhesion. It was determined for the Cr/Au system that the resistivity changes in the gold due to the Cr layer present were significant [7]. It was shown that grain boundary diffusion resulted in the resistivity of the films increasing by much as a factor of eight after just a 6-h anneal time at 280°C, precluding Cr for this use. Similar detrimental grain boundary diffusion was found by Christou and Day [8] for the Ta/Au system at temperatures well below 350°C. Contrary to this behavior, Poate et al. [9] found that for the Ti/Au system, the titanium out-diffuses along grain boundaries to the free surface of the gold where it is subsequently oxidized. Because titanium prefers its oxidized state on the surface, a chemical potential sink is created by which continued diffusion is promoted by the maintenance of a titanium concentration gradient.

To determine the minimum titanium thickness for adequate adhesion, substrates were sputtered with Ti/Au/Ti in which 3, 6, 10, and 15 Å of titanium alternately served as the adhesion overcoat. The deposition rate was determined by measuring the sputtering rate for a 500-Å film (with a 60-s predeposition to eliminate transient effects) and assuming a linear deposition rate. The adhesion of a 5000 Å to 5-μm film of deposited SiO₂ was then evaluated by subjecting the samples to forty thermal shock cycles from 77K (liquid nitrogen) to 373K (boiling water.) The wafers were also scored and a tape test performed. The composites in which the thickness of the titanium adhesion layer was 6 Å or greater showed no signs of delamination or cracking. Thus a minimal adhesion layer of 6 Å of titanium was established.

As the chosen adhesion layer is literally a thin film of titanium covering the entire substrate surface, the maximum titanium thickness that would still guarantee electrical isolation of the overcoated signal lines needed to be determined. Numerous parallel gold signal lines with 10-30-μm spacings were fabricated on top of a thick SiO₂ layer and then overcoated with the titanium adhesion layer. The structures, whose adhesion layer overcoats ranged from 10 to 30 Å, were baked at 95°C for 10 min to oxidize the titanium to TiO₂. The electrical resistances between the individual signal lines were measured, from which the conductivity of the various titanium overcoats could be inferred.

The experimental results for the oxidation of the titanium films are shown in Table III. A 10-Å titanium adhesion layer almost completely oxidized to form TiO₂ at room temperature, and provided no conductive path between the signal lines after a 5-min oxidation step at 95°C. A 20-Å titanium adhesion layer also provided no conductive path between the signal lines after a 10-min oxidation step at the same temperature. Titanium overcoats of 30 Å or greater resulted in appreciable amounts of the layer remaining conductive. This precluded the use of 30 Å or thicker titanium adhesion overcoats. The final selection of a 12-Å dielectric adhesion layer provided a film that was twice the minimum thickness needed for adhesion but well below the minimum conductive thickness. Furthermore, MCM's typically used under heating cycles during dielectric deposition that greatly exceed 95°C, guaranteeing complete oxidation of the 12-Å adhesion film.

Additional investigations of titanium thin films have been carried out by Vogt et al. [10] in which the deposition pattern of sputtered titanium was found to follow an island-growth mechanism. Fig. 4 is a scanning tunneling microscope (STM) image of a sputtered titanium film showing the island-like deposition features. Moreover, Vogt et al. corroborated the assertion that the titanium films do attain a conductive nature at 20–30Å. It was found that for the thinner films the islands began to coalesce and a layer of conductive titanium remained under the insulatory TiO₂. It was suggested that the titanium films have three layers: a titanium core, a suboxide middle layer, and an oxide surface layer, providing a description of how the adhesion mechanism functions. The titanium metal base layer achieves intimate contact with the gold substrate. Since the TiO₂ is grown at or near room temperature, no oxide flaking or oxide/metal separation occurs on the titanium. Finally, insulators can form intimate contact with the TiO₂ on the surface, providing the desired adhesion of the dielectric to the gold metallization.

C. Cost Characterization

The perceived drawback to gold metallization for MCM's has been the materials' cost associated with the gold itself. A cost analysis of these MCM structures demonstrates that noble metal MCM's can actually be manufactured at lower...
costs than some copper processes. Because there are numerous alternatives in the fabrication of copper MCM's, a generic comparison will be made for the purpose of this discussion.

Today, high density MCM-D cost targets are about 20/\text{in}^2 with a near term goal of 10/\text{in}^2 [11]. Using conservative estimates, the metallization materials cost for a typical 4-layer structure using gold is about $1/\text{in}^2$. This is based on a 330/oz. cost of bulk gold, a 20% purification cost, and 2.2 $/\text{in}^2$ of gold metal per square inch of MCM at a thickness of 3 \text{\mu m}. The material cost of the insulator can be an even greater expense than that of the metallization. The cost of a spin-coated organic insulator in Table I can range from $0.60-2.50/\text{in}^2$ for the 4-layer MCM, assuming a 5-\text{\mu m} thickness and 80% loss during spin-on. In comparison, 4 layers of SiO$_2$ can be deposited at a materials cost of approximately $0.10-0.30/\text{in}^2$, depending upon specific facilities and substrate sizes. In any case, the material cost of the dielectric layers will be equal for any MCM metallization process, and for further calculations a value of $1/\text{in}^2$ will be assumed. Similar estimates can be performed to show that substrate costs will range from $0.60-1/\text{in}^2$, assuming the use of either 100- or 200-mm diameter silicon wafers.

Thus the material costs (substrate, gold, dielectric) for a 4-layer MCM-D process are approximately $3/\text{in}^2$. If the cost of labor, equipment, and secondary materials is the same for each layer, it follows that the fabrication cost (total cost minus materials cost) of a 4-layer structure will be $16-18/\text{in}^2$. Thus the fabrication costs alone (processing, equipment, labor, etc.) will be approximately 80-90% of the total cost of an MCM, again based on a total cost of $20/\text{in}^2$. In other words, the $1/\text{in}^2$ material expense of the gold metallization in the entire structure represents only about 2.5-5% of the total MCM cost.

Furthermore, in copper structures a final bond pad layer is added in order to terminate the structure with a bondable metal (i.e., gold). However, with gold metallization, the final bond pad layer is no longer necessary as soldering directly to the top gold metallization layer poses no problems. This eliminates approximately 1/9th of the fabrication costs, leaving eight remaining layers to be fabricated — 4 layers of metal, 4 layers of insulator — and saving $2/\text{in}^2$ in fabrication costs. This 11% reduction in cost is similar to the 8% surface metallization expense suggested by Neuhaus in his MCM-D cost model [12]. Thus with gold metallization, twice the equivalent material cost of the gold in the entire structure is recouped from the elimination of this bond pad layer.

Less tangible, but just as relevant to the cost concerns associated with gold metallization, is the increase in yield that will likely result from the use of gold metallization. The yield of an MCM fabrication process can be described using a clustered defect model

$$Y_T = \left(1 + \frac{D_o A}{\alpha}\right)^{-\alpha}$$

(2)

where $Y_T$ is the yield of any process step, $A$ is the area on the MCM susceptible to the defect, $D_o$ is the defect density, and \alpha is the defect cluster parameter [13]. This cluster parameter is typically equal to 1, whereby (2) reduces to $(1 + D_o A)^{-1}$.

Since the overall yield is simply the product of the yield from each step, it is clear that $Y_T$ will suffer tremendously as both the area of the MCM and the number of processing steps increase.

For example, in a typical copper process many MCM fabricators deposit a 1000 - 10 000 A layer of a barrier metal such as titanium, nickel, or chromium on all exposed surfaces of the copper. This barrier layer serves to promote adhesion between the metal and polyimide as well as to counteract the deleterious effects of the polyamic acid and 2-4% water content present in some polyimides [1]. This process sometimes involves the electroless deposition of metals, which adds at least a total of four processing steps, one for each metal layer. In other cases the copper is lithographically patterned with a barrier metal, adding somewhat more than four processing steps total, again one step per metal layer.

Of course, gold metallization does not require the application of a barrier metal. Assuming a yield of 95% from each processing step, a fabrication process for gold consisting of 28 steps would give a total yield of 24%. A similar copper process consisting of 32 steps (an increase of 4 steps due to the application of a barrier metal) would have a total yield of 19%. Thus a 25% increase in the number of processing steps will result in a 20% lower yield. Lower yields on individual processing steps, such as the electroless deposition of the corrosion protection layers, would only magnify this overall yield difference between otherwise identical copper and gold processes.

IV. CONCLUSIONS

Using standard techniques derived from the semiconductor, printed circuit, and hybrid circuit industries, a fabrication process has been developed to fabricate MCM's utilizing gold metallization. The main concerns involving gold metallization to date have been adhesion difficulties and material costs. The adhesion concerns with gold metallization have been addressed using a low-cost, reliable, easily deposited blanket adhesion layer of TiO$_2$. The material cost concerns with gold metallization have been offset by the reduction in the number of processing steps as well as by recognizing that the majority of the cost for MCM's stems from the fabrication process. In addition, the gold metallization displays a residual stress similar in magnitude to other metals while maintaining the largest portfolio of potential dielectric materials.

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REFERENCES

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