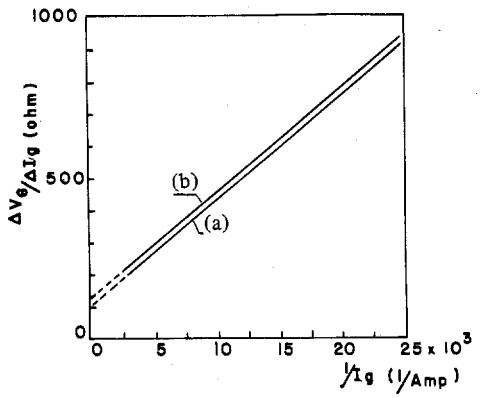

Fig. 4. dV_{gs}/dI_g versus $1/I_g$. (a) Source grounded, drain floating. (b) Drain grounded, source floating.

$R_{ch}/2 = 102.6\ \Omega$ and $R_d + R_{ch}/2 = 126.3\ \Omega$. Hence, $R_s = 42.2\ \Omega$, $R_d = 65.8\ \Omega$ and $R_{ch} = 121\ \Omega$.

The measured dV_{gs}/dI_g versus $1/I_g$ curves for both configurations are shown in Fig. 4. The intercepts of these curves yield $R_s + R_{ch}/2 + R_g = 107\ \Omega$ and $R_d + R_{ch}/2 + R_g = 129\ \Omega$. Hence, $R_d - R_s = 22\ \Omega$, in excellent agreement with our "end" resistance measurements. The value of R_g is approximately 4 Ω.

We also measured V_{ds} versus I_d for $I_g = 500\ \mu A \gg I_d$. This curve is practically linear with the slope $R_s + R_d + R_{ch} = 224\ \Omega$ in a good agreement with the "end" resistance measurement ($R_s + R_d + R_{ch} = 228.9\ \Omega$).

These results show that the "end" resistance measurements, interpreted using (11), allow an accurate determination of the series source and drain resistances.

ACKNOWLEDGMENT

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Photoelectrochemical Plating of Via GaAs FET's

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Abstract—**A new photoelectrochemical (PEC) technique for filling via holes in GaAs FET's with a solid deposit of metal, such as gold, has been developed. Photogenerated electrons reduce solvated $Au(CN)_2^-$, directly on the FET source pads, allowing narrow straight-walled plasma-etched via holes to be filled without forming voids. The photogenerated holes cause the decomposition of a small amount of the semi-insulating (SI) substrate. With illumination from a 1200-W tungsten-halogen lamp, plating rates of 0.8 μm/min over a 2-in-diam wafer are achieved. The plating rate is insensitive to $Au(CN)_2^-$ concentration in the range 0.01 to 0.15 M. The resulting GaAs FET's show improved mechanical stability and thermal resistance.**

GaAs FET's with via connections through the substrate to the source pads have higher gain at microwave frequencies, higher power density, and potentially lower manufacturing costs than conventional GaAs FET's [1], [2]. Initially, the via holes were formed by chemical etching. This resulted in wider than necessary holes because of the lateral etching of the isotropic chemical etch. Recently, plasma etching has been used to anisotropically etch via holes with straight sides [2] resulting in a higher transistor packing density.

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It is more difficult to fill these narrow straight-sided holes with metal than to fill the wider chemically etched holes. The via holes cannot be electroplated by conventional means because it is not possible to make direct electrical connection to the source pads. The usual procedure is to deposit a thin layer (~1 μm) of electroless gold on the base of the substrate including the walls of the via holes and the source pads. The thickness of the gold is then increased by electroplating. The current density at the bottom of the narrow via holes is much lower than the top and the resulting void under the source pad can cause mechanical, thermal, and reliability problems.

In this paper, a new photoelectrochemical (PEC) technique is described for depositing gold or other metals directly on the source pads without the need for electrical contact. Light induces the dissolution of the GaAs substrate and the deposition of gold. The metal plates only on the source pads, filling the via holes with a solid structure of gold. Significant improvements in the thermal resistance and mechanical stability of the FET's have been obtained [3].

The FET wafer is mounted with the device side waxed to a sapphire disk so that only the semi-insulating (SI) substrate and the gold source pads at the bottom of the via holes are

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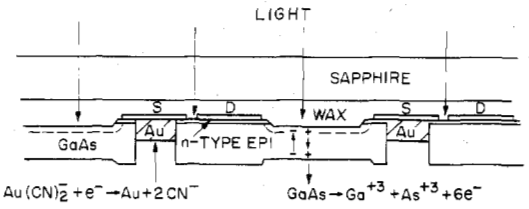

Fig. 1. Diagram of the plasma-etched via GaAs FET mounted on a sapphire substrate. The chemical reactions which take place during plating are shown.

exposed to the plating solution. The arrangement is illustrated by the cross-sectional diagram in Fig. 1. The substrate is cleaned to remove any gold residues resulting from the plasma etching and then etched in a $H_2SO_4/H_2O_2/H_2O$ solution.

For gold deposition, the wafer is then immersed in a phosphate buffered aqueous potassium gold cyanide solution and uniformly irradiated using a tungsten-halogen lamp.

The irradiation generates electron-hole pairs which are separated by the space-charge field in the SI GaAs. The width of the space-charge region in SI GaAs is much greater than the 30-μm substrate thickness so that the field is present throughout the substrate. The photogenerated holes drift to the GaAs solution interface where they cause decomposition of the semiconductor by the reaction [4]

$$GaAs + 6h^+ \rightarrow Ga(III) + As(III). \quad (1)$$

The Ga(III) and As(III) undergo further chemical complexation and their final form is dependent upon the pH [5].

The photogenerated electrons drift to the device side of the wafer where they reduce the solvated $Au(CN)_2^-$ complex on the gold source pads by the reaction

$$Au(CN)_2^- + e^- \rightarrow Au + 2CN^-. \quad (2)$$

Reduction does not occur on the exposed n-GaAs layer because of the depletion region formed at the semiconductor/solution interface. Fig. 2 is an SEM photomicrograph of a gold deposit attached to a transistor source pad with the GaAs substrate etched away. The sides of the deposit closely conform to that of the via hole. The best results are obtained when the wafer is illuminated on the device side as shown in Fig. 1. When illuminated on the substrate side, many wafers showed a tendency for gold to deposit in irregular patterns on the GaAs substrate. This surface plating is probably caused by the high concentration of photogenerated electron-hole pairs which are separated in the local electric fields near surface defects or strained regions opposite the device metallizations. The irregular plating and etching of the surface then proceeds as explained. The resultant plated gold is poorly bonded to the GaAs surface. When the wafers are irradiated from the device side, most of the light is absorbed near the surface where the photogenerated carriers form an equipotential conducting layer between the mesas.

The potential for the photoassisted dissolution of SI GaAs in (1) is more negative than for the reduction of gold cyanide in (2) by about 0.25 V, thus an exothermic reaction occurs.

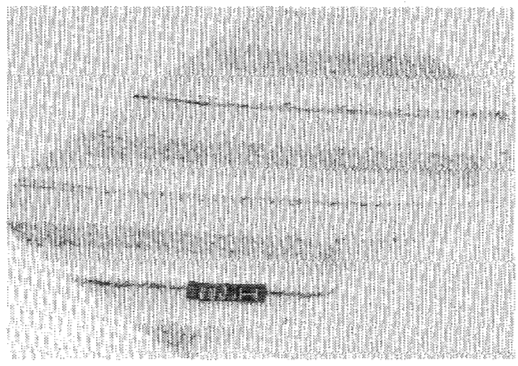

Fig. 2. Scanning electron micrograph of the photoelectrochemically plated gold after removal of the GaAs substrate.

The reduction potential for (1) and (2) both have a 58-mV/pH dependence so that the driving force for the reaction is uniform over a wide pH range. The plating rate is slightly lower around pH 7 due to the lower solubility of the Ga and As oxides. Since the GaAs area and volume are much larger than the amount of gold plated, (1) consumes only an insignificant amount of GaAs, usually <1 μm of a 30-μm-thick wafer. The area of the via hole was 6×10^{-4} mm^2.

Experiments in which the spectrum of the radiation from the tungsten lamp was changed with color filters have indicated that the plating rate depends only on the spectral intensity in the vicinity of the GaAs absorption edge. A measurement of the quantum efficiency (tungsten-halogen lamp), with which photons that are absorbed by the GaAs, produce deposited gold gave a value of only 0.3 percent after appropriate corrections for reflectivity and the fraction of the surface covered by the metal. Such a small value is understandable if only that small fraction of the spectrum in the vicinity of the absorption edge is utilized in plating.

Radiation near the absorption edge generates carriers throughout the substrate which assists the transport between the substrate surface and the source pads. This indicates that the rate of arrival of carriers at the liquid junction interface is the rate-limiting process for the plating.

The plating rate approximately doubles for every 10°C increase in temperature over the range 25 to 65°C. Although this is typical of chemical reaction rates, it is also about the rate at which the carrier concentration should increase in intrinsic GaAs. The plating rate was independent of $Au(CN)_2^-$ concentration over the range from 0.01 to 0.15 M, again indicating the carrier dependence.

GaAs FET's, with via holes PEC plated half full, have been thermally aged at 250°C for greater than 1000 h and no deformation of the source pads has been observed. Also, there is no evidence of tin diffusion into the source pads from the braze material. Thermal resistance measurements of photoelectrochemically plated vias show values unchanged from conventional nonvia GaAsFETs [3], [6]. In contrast, via-transistors made without PEC plating show thermal resistance values as much as 33 percent higher than nonvia devices.

The PEC technique described in this paper allows narrow plasma-etched via holes to be filled with a solid deposit of gold. The deposition of gold is insensitive to solution pH and

$Au(CN)_2^-$ concentration over a wide range. With a 1200-W tungsten-halogen lamp plating rates of 0.8 μm/min over a 2-in-diam wafer are achieved allowing the via holes to be filled in approximately 0.5 h. The resulting devices show improved mechanical stability and thermal resistance.

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Deep-Level Analysis in (AlGa)As–GaAs 2-D Electron Gas Devices by Means of Low-Frequency Noise Measurements

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Abstract—**Low-frequency noise of (AlGa)As–GaAs heterostructures grown by molecular-beam epitaxy was investigated. The temperature of the samples was varied between 100 and 400 K. In the frequency range from 1 Hz to 25 kHz noise spectra can be described as superposition of several generation-recombination (GR) noise components. Four deep levels (E = 0.40, 0.42, 0.54, 0.60 eV) were detected, three of which are in agreement with those measured independently by deep-level transient spectroscopy (DLTS).**

I. INTRODUCTION

AN IMPORTANT PROGRESS in the development of microwave and high-speed electron devices was the discovery of a quasi two-dimensional electron gas (TEG) located at the interface of certain semiconductor heterostructures [1]. The system (AlGa)As-GaAs is used for fabricating field-effect transistors (FET's) which are called two-dimensional electron gas FET's (TEGFET's) [2], high electron mobility transistors (HEMT's) [3] or modulation-doped FET's. (MODFET's) [4]. Electrons are transferred from the n-doped (AlGa)As into the undoped GaAs and form the TEG near the interface. Therefore ionized donors and free electrons are spatially separated and the Coulomb scattering is reduced. Very high mobilities result especially at lower temperatures.

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The deep-level characteristics of the heterostructure are important, since electron traps reduce carrier concentration and mobility and increase noise. They can be characterized by low-frequency noise measurements. Generation-recombination (GR) noise is caused by fluctuation in the number of free electrons. Discrete energy levels in the forbidden gap are able to trap electrons or act as recombination centers. Theory explains that these fluctuations cause Lorentzian shaped GR noise contributions in the specturm of ac open-circuit voltage noise [5], [6]. Each trap has a characteristic spectrum defined by its low-frequency plateau value (amplitude) and the corner frequency, from the variation of which, with temperature, the activation energy of the deep level is deduced. The trap concentration is related to the amplitude. Only levels not more than a few kT away from the Fermi level contribute to noise. By changing the temperature the Fermi level is shifted across the forbidden gap.

II. EXPERIMENTAL PROCEDURE

Two types of heterostructures grown by MBE were investigated (Table I). Their main difference is the spacer layer of undoped (AlGa)As in sample D1 which enhances the mobility of the two-dimensional electron gas.

A test pattern allowed the measurement of electron Hall mobility and contact resistance from a transmission-line structure. For the noise measurements the samples consisted of two ohmic contacts with 60-μm separation and 100-μm contact width. Ohmic AuGe/Ni contacts with a specific contact resistance of about 10^{-4} Ω·cm^2 were used.

Samples were mounted in a cryogenic system allowing

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