Abstract—This paper discusses the design, fabrication, and characterization of packaged planar inductors with magnetic material [nickel zinc (NiZn) ferrite]. Inductors are designed specifically for Internet of Things (IoT) applications based on power loss in an IoT architecture. Different spiral inductor geometries are demonstrated on a printed wiring board with varying thicknesses using a stencil printing process. The magnetic material can be applied to one or both sides of the inductor and, therefore, provides size reduction. This paper examines the role of varying dimensions on inductor performance along with model-to-hardware correlation. The fabrication process demonstrates inductance increase through a very simple procedure for applying a magnetic material on both sides of the inductor, while having flexibility to customize the geometry for minimal power loss in an IoT architecture. With NiZn ferrite material added to both sides of the inductor, the inductance increases between approximately 60% and 80% for the two substrate thicknesses studied, as compared to air-core inductors.

Index Terms—DC–DC power conversion, embedded inductors, magnetic materials, packaging.

I. INTRODUCTION

IN AN increasingly internet-connected society, the number of devices per person is already more than one and will increase further. This provides great potential for Internet of Things (IoT) applications, including edge devices. Edge devices may be placed in diverse locations, needing to rely on either stored power [1] or harvested power [2]. An IoT system operates at lower supply voltage and power than most applications utilizing a power IC, and therefore, power efficiency is a high priority. Since the desired power source may deliver power inconsistently, dc–dc converters should have high efficiency while operating at discontinuous (or burst) mode under various loading conditions [3]–[5]. Due to this, switching regulators are used for dc–dc conversion instead of linear regulators. Since switched capacitor converters’ efficiency decreases during regulation, switched inductor converters are preferred for the power management of IoT devices [6].

In switched inductor dc–dc converters, inductors are the key power transfer elements [7]–[9], and therefore, optimizing their design for maximum performance is necessary [10]–[12]. To deliver clean power to the load with high efficiency, the inductor needs to have the right inductance (to minimize current ripple) with minimum loss (both dc and dc).

Discrete chip inductors take up significant area and have large dc resistance [13]. Since IoT applications require small size, inductor integration with small dc resistance is required. Embedded inductors provide miniaturization through size reduction, provide performance enhancements due to lower parasitics, and are often more reliable since they are not assembled on the printed wiring board (PWB). Improved design flexibility is achieved since the inductors can be placed close to the devices. Depending on the geometry, the inductors can be embedded in 2-D form (e.g., planar inductors) [14] or as 3-D structures (e.g., solenoidal inductors) [13] using air or magnetic core.

A commonly adopted 2-D inductor geometry is the spiral since it provides a relatively higher inductance density, is easier to fabricate, and is simpler to design as compared to 3-D inductors. Unlike integration on the chip, PWB integration provides opportunities for reducing cost, provided a simple and cost-effective technique can be developed for the power inductor fabrication. Because edge devices are often used in consumer applications, cost becomes even more critical for an IoT architecture. Our focus in this paper is on the integration of inductors in the PWB with direct chip attach, which we refer to as system-in-package (SiP) technology.

Many SiP implementations of power inductors use an air core. Though creative topologies and geometries may be used to reduce size, area-efficient designs are only possible with the use of magnetic materials since magnetic materials enable inductance increase without a corresponding dc resistance increase. Many recent examples of embedded, planar power inductors exploit magnetic materials. Examples include clean room fabrication process, with screen-printing MnZn [15], PWB etching with screen-printing NiZn ferrite [16], and electroplating between layers of YIG [17]. On-silicon planar inductors for on-chip implementations have also been demonstrated [18]–[22].

Our focus in this paper is the use of the conventional PWB processes for integrating inductors into the PWB at low cost,
which represents the main contribution of this paper. Such an integration allows for an SiP IoT solution, which is in contrast to silicon inductor fabrication, as demonstrated in [18]–[22]. The magnetic composite in this paper has been specifically treated to be FR4-compatible, leading to a higher permeability than reported in [16] with improved adhesion to the substrate. The stencil printing process used is simpler and of comparable quality to other magnetic-layer deposition methods, such as that demonstrated in [19] and [22]. The demonstrated process is applicable to a basic two-layer PWB, but is transferrable to any number of layers, showing more flexibility with fewer fabrication steps than that demonstrated in [16] and [21]. While previously demonstrated stencil-printing fabrication processes have similarities to this paper, we focus on a simple procedure that may be applied to both rigid and flexible substrates with one or two magnetic layers with no increase in fabrication complexity, which represents a key improvement over similar work.

We start by briefly describing the IoT architecture in Section II to determine the inductor requirements by analyzing power losses. In Section III, the inductor geometry and design procedure are presented. Section IV outlines the fabrication process, with Section V providing measurement results, followed by Section VI where the inductors are compared with that of other published work. Finally, we provide the conclusion in Section VII.

II. IoT ARCHITECTURE

The considered IoT architecture is shown in Fig. 1 where near-field coupling at 1 GHz is used as a power source with an input power of 100 mW to provide power to a load in the range of 50 mW, after rectification (50% overall conversion efficiency target). Since the input power has inconsistent voltage, an inductive buck converter with a planar inductor is used for dc–dc conversion and voltage regulation. The needs imposed on the inductor are quite stringent since low dc resistance is required to maximize efficiency. Adding more turns to the inductor or decreasing trace width are the methods to increase inductance density, but these methods increase dc resistance substantially [23]. Therefore, alternate solutions are required for reducing the area.

Using a planar inductor with magnetic material can increase inductance density without sacrificing dc resistance. In the architecture shown in Fig. 1, the operating frequency is 10 MHz for the dc–dc converter. At the considered power levels and operating frequency, poorly designed power inductors will have considerable inductor power losses and lead to degradation in the IoT power efficiency.

There are four main sources of power loss in the IoT system in Fig. 1, namely: 1) loss through near-field coupling; 2) loss during rectification; 3) switching and conduction losses in the converter; and 4) inductor losses.

A typical 1-GHz wireless power transfer module containing RF coils and a full-wave diode rectifier can have considerable losses, so the buck converter and inductor losses need to be minimal. The buck converter chip in Fig. 1 uses the Global Foundries (GF) 130-nm process with a 3-V-input voltage. The chip, discussed in [13], has multiple conversion ratios, where the 3:1-V conversion ratio is used for this paper. The inductor dc \( P_{\text{Ind}(dc)} \) and ac \( P_{\text{Ind}(ac)} \) power losses for the buck converter can be estimated using [13]

\[
P_{\text{Ind}(dc)} = R_{dc} \cdot I_{\text{Load}}^2
\]

\[
P_{\text{Ind}(ac)} = \frac{R_{ac} \Delta I_{\text{pk-pk}}^2}{12}
\]

\[
\Delta I_{\text{pk-pk}} = \frac{(V_{\text{in}} - V_{\text{out}})D}{f_{SW}L}
\]

\[
D = \frac{V_{\text{out}}}{V_{\text{in}}}
\]

where \( R_{dc} \) is the dc resistance of the inductor, \( I_{\text{Load}} \) is the load current, \( R_{ac} \) is the ac resistance of the inductor, \( f_{SW} \) is the switching frequency, \( \Delta I_{\text{pk-pk}} \) is the maximum ripple current, \( V_{\text{in}} \) and \( V_{\text{out}} \) are the input and output voltages for the converter, \( L \) is the inductance, and \( D \) is the duty cycle [24]. Furthermore, the buck converter losses can be estimated using

\[
P_{\text{Buck(Cond)}} = R_{SW}(I_{\text{Load}}^2 + \Delta I_{\text{RMS}}^2)
\]

\[
P_{\text{Buck(Switching)}} = f_{SW} \left[ C_{\text{GSN}} \left( \frac{V_{\text{in}}}{2} \right)^2 + 2C_{\text{GDN}} \left( \frac{V_{\text{in}}}{2} \right)^2 \right] + C_{\text{GSP}} \left( \frac{V_{\text{in}}}{2} \right)^2 + 2C_{\text{GDP}} \left( \frac{V_{\text{in}}}{2} \right)^2 \]

\[
\Delta I_{\text{RMS}} = \frac{\Delta I_{\text{pk-pk}}}{2\sqrt{3}}
\]

where \( P_{\text{Buck(Cond)}} \) is the conduction loss in the buck converter transistors, \( P_{\text{Buck(Switching)}} \) is the buck converter switching losses calculated using the various gate capacitances with \( C_{\text{GSN}} = 0.813 \text{ pF} \), \( C_{\text{GDN}} = 0.583 \text{ pF} \), \( C_{\text{GSP}} = 0.71 \text{ pF} \), and \( C_{\text{GDP}} = 0.59 \text{ pF} \), and \( R_{SW} \) is the resistance of the transistor switches [13]. For the GF 130-nm process, the transistor resistances and capacitances were modeled for \( V_{\text{in}} = 3 \text{ V} \), \( V_{\text{out}} = 1 \text{ V} \), and output power of 50 mW. The quality factor \( Q \) for an inductor can be defined as

\[
Q = \frac{\alpha L}{R_{AC}}
\]

where the \( Q \) factor takes into account both the winding and core losses. At 10 MHz, and assuming a quality factor
of 25 and a dc resistance of 600 mΩ for the inductor, an efficiency in the range of 82%–92% is possible for inductances in the range of 200–800 nH, as shown in Fig. 2. In this paper, our focus is on the design, fabrication, and characterization of embedded planar power inductors, where the inductance is in the range of 200–800 nH, as shown in Fig. 2. In this paper, as a comparison, three structures have been designed and fabricated as shown in Fig. 3(c): air-core inductor, single-layer magnetic material inductor (on one side of the PWB), and two-layer magnetic material inductor (on both sides of the PWB).

III. SPIRAL INDUCTOR DESIGN

A. Spiral Inductor Geometry

Planar spiral inductors have been shown to provide high inductance density and, hence, have been used in this paper, as shown in Fig. 3(a). The critical design parameters are the outermost length \( d \), metal trace width \( w \), the trace separation \( s \), and the number of turns \( N \). The inductor is designed on a two-layer PWB core of thicknesses 0.79 and 0.2 mm, as shown in Fig. 3(c), where the 0.2-mm thickness makes the substrate flexible. The inductor windings are defined on the top, while a ground plane is provided on the bottom layer with an opening cutout in the ground plane beneath the inductor, as shown in Fig. 3(b). The cutout helps increase the inductance and \( Q \) factor of the inductors, leading to reduced area and losses.

The magnetic material is applied to one or both sides of the inductor. For the double-sided case, inductance is increased over the single-sided case due to the presence of the magnetic field in the magnetic material on both sides of the inductor. As a comparison, three structures have been designed and fabricated as shown in Fig. 3(c): air-core inductor, single-layer magnetic material inductor (on one side of the PWB), and two-layer magnetic material inductor (on both sides of the PWB).

B. NiZn Ferrite Magnetic Material

At 10 MHz, the magnetic material can introduce additional ac losses. The magnetic material used in this paper is a NiZn ferrite epoxy composite with a volume loading of 0.78, with details available in [25]. The magnetic composite was prepared by mixing NiZn ferrite powder (FP 350 from pptechnology) with epoxy polymer, with the powder physical and electrical characteristics supplied in [26]. Acetone was used as the solvent, and the viscosity of the paste for stencil printing was tuned by adjusting the ratio of solvent to the magnetic composite. To accurately model the inductor, the electromagnetic properties of the magnetic material are required. The properties of the magnetic material were obtained using a 4291B RF Impedance/Material Analyzer with the 16454A Magnetic Material Test Fixture and the 16453A Dielectric Material Test Fixture, from Keysight. The measured permeability and permittivity spectra of the NiZn ferrite composite magnetic material up to 100 MHz are shown in Fig. 4. The composite has a relative permeability of 9.3, magnetic loss tangent of 0.25, relative permittivity of 6.3, and dielectric loss tangent of 0.01 at a frequency of 10 MHz, which corresponds to the switching frequency in this paper.

C. Spiral Inductor Design and Modeling

The inductors were designed using ANSYS HFSS v17.1, a full-wave electromagnetic simulator, to accurately estimate the ac losses at 10 MHz. FR4 material \( (\epsilon_r = 4.5 \text{ and } \tan(\delta) = 0.02) \) was used as the substrate to ensure low cost with thicknesses of 0.2 and 0.79 mm. The copper traces have a thickness of 35 \( \mu \text{m} \) with trace width \( (w) \) and spacing \( (s) \) ranging from 100 to 250 \( \mu \text{m} \). As seen in the inductor-side cross section in Fig. 5, the application of magnetic material concentrates the magnetic field strength in the area of the inductor for increased inductance.

For initial simulations, a magnetic material thickness of 50–600 \( \mu \text{m} \) (air core) was used consistent with the thicknesses attained by the stencil printing process (50–600 \( \mu \text{m} \) described in Section IV. Fig. 6 shows the effect of the magnetic layer thickness and the substrate thickness on the inductance and resistance at 10 MHz. For a spiral geometry of \( d = 7.5 \text{ mm}, \ w = 0.15 \text{ mm}, \ s = 0.20 \text{ mm}, \text{ and } N = 7 \), the magnetic layer thickness on both the top and bottom layers was swept for both 0.79- and 0.2-mm-thick PWBs. As the magnetic layer thickness increases, both the inductance and the ac resistance increase, as expected. For the 0.2-mm-thick flexible substrate, the inductance and resistance increase is more significant due to the decreased distance between the bottom magnetic layer and spiral inductor. Since
the core losses in the inductor must be carefully balanced with the inductance increase, a target magnetic layer thickness of 200–400 μm is desired. The inductance and inductance density are less than desired with less than 200-μm thickness, and the quality factor can fall below 25 with greater than 400-μm thickness. This magnetic-layer thickness range has sufficiently small ac resistance to have allowable quality factor for both substrate thicknesses while significantly increasing inductance from the magnetic layer.

Magnetization measurements were performed on the NiZn ferrite epoxy composite, and the results showed that magnetic composite material saturates at 0.13 T. From $B = \mu H$, with the saturating magnetic flux density $B$ and permeability $\mu$ already known for the material, an HFSS simulation of the magnetic field strength as a function of inductor current can provide an estimate of the saturation current. This is shown in Fig. 7, where the inductor 1 geometry was simulated with a top magnetic layer of 0.3-mm thickness for varying current excitations. The magnetic field strength does not reach the saturation condition until approximately 1.5 A, which is far greater than the currents typical for these low-power applications. Thus, we can assume the magnetic core will not saturate for the normal operation of these inductors.

Based on simulations and requirements, five inductors were designed, with geometries defined in Table I. Each design was simulated with zero, one, and two magnetic layers and with
TABLE I
SPIRAL INDUCTOR GEOMETRIES

<table>
<thead>
<tr>
<th>Inductor#</th>
<th>d (mm)</th>
<th>w (mm)</th>
<th>s (mm)</th>
<th>N turns</th>
<th>$R_{dc}$ (mΩ)</th>
<th>$L (nH)$</th>
<th>Peak Q</th>
<th>Peak Q Freq (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5.94</td>
<td>0.23</td>
<td>0.23</td>
<td>5</td>
<td>171</td>
<td>200</td>
<td>27</td>
<td>12</td>
</tr>
<tr>
<td>2</td>
<td>5.94</td>
<td>0.15</td>
<td>0.15</td>
<td>6</td>
<td>337</td>
<td>374</td>
<td>26</td>
<td>14</td>
</tr>
<tr>
<td>3</td>
<td>8.38</td>
<td>0.23</td>
<td>0.23</td>
<td>7</td>
<td>333</td>
<td>436</td>
<td>29</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>7.47</td>
<td>0.23</td>
<td>0.23</td>
<td>6</td>
<td>261</td>
<td>341</td>
<td>29</td>
<td>13</td>
</tr>
<tr>
<td>5</td>
<td>7.47</td>
<td>0.15</td>
<td>0.15</td>
<td>7</td>
<td>506</td>
<td>608</td>
<td>28</td>
<td>14</td>
</tr>
</tbody>
</table>

0.2- and 0.79-mm substrate thicknesses to determine the effect of NiZn ferrite composite on inductance density and magnetic losses in the inductor. The dc resistance of the inductor was calculated using (9), while the inductance and $R_{ac}$ values were extracted from simulations at 10 MHz with 200-μm-thick magnetic layers on the top and bottom, where $N$, $d$, $w$, and $s$ are as described in Fig. 1 and $\rho_{copper}$ is the resistivity of copper [27]

$$R_{dc} = \frac{\rho_{copper} (4Nd - 4N^2w - (2N - 1)^2s)}{w \text{(thickness}_{copper})}.$$  (9)

IV. FABRICATION OF INDUCTORS

The fabrication process for the inductor is shown in Fig. 8. Starting with a basic two-copper-layer FR4 PWB, the top and bottom copper layers are etched, creating the inductor pattern and the cutout/trench, respectively, as shown in Fig. 8(a). The patterned planar inductors and trenches are shown in Fig. 8.

The copper trace width and separation were measured using an optical microscope. The copper trace thickness and trench depth were obtained using the Veeco Dektak 150 surface profilometer. The copper trace thickness was around 42 μm, and the trench depth was 35 μm for the inductors.

The top magnetic layer was deposited with the NiZn ferrite composite using stencil printing (MPM SPM 7279 Semiautomatic Stencil Printer), as shown in Fig. 8(b). The board was designed symmetrically so the same stencil could be used for the top and bottom layers’ deposition. Alignment marks on the stencil and the board ensured that the magnetic material was placed precisely on the inductor.

The boards were cured for 1 at 180 °C to form the top magnetic composite core. To prevent the creation of air bubbles, the curing temperature increased gradually up to the final temperature. For depositing the second magnetic layer, the same stencil screen and magnetic paste are used. The bottom magnetic layer was stencil-printed, and the boards were cured again for 1 at 180 °C to form the bottom magnetic composite layer, as shown in Fig. 8(c).

A fabricated inductor and the thickness of the magnetic layers on the inductor measured using the profilometer are shown in Fig. 10. In addition to providing a low-cost method for applying magnetic layers to both sides of the PWB, a key advantage of this process is ease of integration in an SiP solution for IoT applications. Since the spiral inductors can be co-designed and fabricated with the rest of the IoT system,
an optimum design is possible, thereby enabling a higher power efficiency.

V. EXPERIMENTAL RESULTS

A. Inductor Measurement Procedure

The fabricated inductors were measured between 10 and 50 MHz using an Agilent H8363B Vector Network Analyzer, calibrated using SOLT standards. One-port S-parameters were measured and subsequently converted to Z-parameters. The inductance and \( Q \) were extracted using

\[
L = \frac{\text{Im}(Z_{11})}{\omega} \tag{10}
\]

\[
Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \tag{11}
\]

for a frequency range between 10 and 50 MHz, where \( Z_{11} \) is the Z-parameter converted from the measured S-parameter. The inductance of the feedline/SMA connector was also measured and de-embedded, which had an inductance contribution of 6–8 nH for the various line widths used in the designs.

B. Measurement Results

Fig. 11 shows the measurement results for inductor design 4, showing the comparison of inductance and quality factor between the different cases. For this comparison, all designs had the same spiral geometry and a trench in the ground plane, where the rigid substrate has thickness 0.79 mm and the flexible substrate has thickness 0.20 mm. At 15 MHz, inductor 4 has an inductance increase from 194 to 268 nH from the application of a single magnetic layer on the top layer of the inductor—an increase of over 30%. At lower frequencies, the \( Q \) factor is higher for the single magnetic layer case compared to that of the air-core case since the increase in inductance is much larger than the increase in resistance. At higher frequencies, however, the \( Q \) factor reduces because the loss tangent of the magnetic material increases with frequency while the permeability does not, as shown in Fig. 4. The peak \( Q \) occurs between 10 and 20 MHz.

For the rigid substrate with double magnetic layer, the inductance increases to 310 nH, which corresponds to a 60% inductance increase over the air-core inductor. The \( Q \) factor has similar values as the single magnetic layer near the frequency of operation, and therefore, ac losses are not significantly increased.

For the double-sided magnetic layer on flexible substrate, the inductance measured was 351 nH for inductor 4. This inductance increase as compared to the rigid substrate can be attributed to the increased magnetic field density in the inductor due to the reduced substrate thickness. However, the higher magnetic field density results in increased magnetic losses that affect the quality factor of the inductors. As shown in Fig. 11, the quality factors are still above 25 and remain large enough to maintain the \( R_{ac} \) losses for the power inductor below the required value.

C. Simulation Correlation

Based on the measurement results in Section V, the inductors were remodeled using the electromagnetic simulator ANSYS HFSS v17.1 by accounting for the measured thickness for the magnetic material to obtain good model-to-hardware correlation. Here, we only examine inductors 1 and 5 as examples. Using a one-port simulation, the self-impedance was calculated from the S-parameter \((S_{11})\). The self-impedance provides the frequency response of the inductance loop, from which the inductance and \( Q \) factor can be extracted using (10) and (11).

The inductance comparison between simulation and measurement results for the 0.2- and 0.79-mm-thick boards is...
shown in Fig. 12. The simulations slightly overestimate the inductance, which can be attributed to the fabricated magnetic layers having minor air pockets after curing, which were not included in the simulations. As mentioned earlier, the magnetic thickness was modeled as an average thickness in HFSS based on measurements, accounting for some variation in the inductance and quality factor.

VI. INDUCTOR COMPARISON

All five inductor geometries were measured with no magnetic layers, with only a top magnetic layer, and with magnetic layers on the top and bottom. The measurement results for all seven inductor designs show similar trend as the data shown for inductor 4, and these results are listed in Table II. For all seven designs, the inductance showed significant increase from the application of NiZn ferrite magnetic layer(s). As expected, the 0.2-mm substrate with double magnetic layers had the largest overall inductance, significantly increasing the inductance over the air-core inductor without increasing the dc resistance. The fabricated inductors also compare favorably with other implementations of PWB compatible planar inductors with magnetic layers published in the open literature, as shown in Table III. While the electrical properties of the spiral inductor in [15] are suitable, the area is larger as compared to this paper. Details provided in [21] and [22] have the desired electrical properties for an IoT solution with good area efficiency, but are on-chip implementations. In general, on-chip implementations for the inductors with magnetic material require a more expensive process and use additional chip area. While much higher inductance densities have been demonstrated, as listed in [28], they do not utilize processes outside a clean room, as shown in this paper. The process in [16] involves more steps and layers, leading to a much larger dc resistance and subsequently much higher dc inductor loss.

Unlike SMT inductors, which are discrete, the power inductors described in this paper can be custom designed for obtaining the optimum efficiency for a variety of IoT applications. Fig. 13 shows the modeled efficiency of the 10-MHz buck converter using the measured data for the double-sided, 0.20-mm-substrate-thickness inductor for all the designs discussed. The modeled efficiency is between 85%–94%. The breakdown of losses for the buck converter for inductor 5, double-sided 0.2-mm thickness at 10 MHz

TABLE II

<table>
<thead>
<tr>
<th>Inductor</th>
<th>Air Core Inductance</th>
<th>Air Core Peak Q</th>
<th>Single Magnetic Layer</th>
<th>Single Magnetic Layer Peak Q</th>
<th>0.79 mm Two Magnetic Layers</th>
<th>0.79 mm Two Magnetic Layers Peak Q</th>
<th>0.2 mm Two Magnetic Layers</th>
<th>0.2 mm Two Magnetic Layers Peak Q</th>
<th>Peak Q (MHz)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>109 nH</td>
<td>26</td>
<td>145 nH</td>
<td>36</td>
<td>182 nH</td>
<td>40</td>
<td>201 nH</td>
<td>26</td>
<td>14</td>
<td>35.33</td>
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<td>2</td>
<td>201 nH</td>
<td>27</td>
<td>258 nH</td>
<td>33</td>
<td>293 nH</td>
<td>34</td>
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<td>3</td>
<td>271 nH</td>
<td>32</td>
<td>374 nH</td>
<td>38</td>
<td>439 nH</td>
<td>37</td>
<td>501 nH</td>
<td>34</td>
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<td>70.26</td>
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<td>4</td>
<td>194 nH</td>
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<td>268 nH</td>
<td>41</td>
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<td>39</td>
<td>351 nH</td>
<td>32</td>
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<td>55.77</td>
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<tr>
<td>5</td>
<td>334 nH</td>
<td>32</td>
<td>468 nH</td>
<td>36</td>
<td>552 nH</td>
<td>38</td>
<td>696 nH</td>
<td>31</td>
<td>14</td>
<td>55.77</td>
</tr>
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</table>

TABLE III

<table>
<thead>
<tr>
<th>Comparison With Other Inductors</th>
<th>This Work</th>
<th>[15]</th>
<th>[16]</th>
<th>[21]</th>
<th>[22]</th>
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</thead>
<tbody>
<tr>
<td>Inductor Fabrication</td>
<td>PWB Etch</td>
<td>Photo-</td>
<td>PWB</td>
<td>In-Silicon</td>
<td>In-Silicon</td>
</tr>
<tr>
<td>Magnetic Application</td>
<td>Screen Printing</td>
<td>Screen</td>
<td>Printing</td>
<td>Screen Printing</td>
<td>Manual Pressing</td>
</tr>
<tr>
<td>Magnetic Thickness (mm²)</td>
<td>506</td>
<td>15</td>
<td>&gt;2000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance (nH)</td>
<td>696</td>
<td>150</td>
<td>810</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Q</td>
<td>31</td>
<td>20</td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductance Density (nH/mm²)</td>
<td>12.5</td>
<td>.7</td>
<td>33.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>55.77</td>
<td>225</td>
<td>24.44</td>
<td></td>
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</tr>
<tr>
<td>Frequency (MHz)</td>
<td>15</td>
<td>1</td>
<td>10</td>
<td></td>
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</tbody>
</table>

*Estimated from (9) and dimensions reported in [16]
is shown in Fig. 14, where inductor’s ac and dc losses contribute 45% and 10% of the total power losses. This compares to 45% of the power losses arising from the FET transistor losses (conduction and switching).

VII. CONCLUSION

Power inductors have been designed, fabricated, and characterized in this paper specific to the needs of an IoT architecture. To investigate inductor performance, different geometries and substrate thicknesses were used in the PWB inductor design. Using stencil printing with NiZn ferrite magnetic composite material on both sides of a PWB, the inductance of the spiral inductor was shown to increase by up to 80%, as compared to the inductors without the magnetic layer. This fabrication process is amenable to both rigid and flexible substrates with single or double magnetic layers, yielding improved design flexibility for a variety of IoT applications. The inductors shown in this paper are suitable for use with buck converters in IoT architectures switching at 10 MHz, with efficiencies of 90%.

REFERENCES


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Shinji Nakazawa, photograph and biography not available at the time of publication.