Design, Fabrication, and Characterization of Package Embedded Solenoidal Magnetic Core Inductors for High-Efficiency System-In-Package Integrated Voltage Regulators

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In this paper, we discuss the design, fabrication, and characterization of package embedded solenoidal inductor using a NiZn ferrite magnetic core material based on the novel fabrication process. The process relies on stencil printing of the magnetic core material along with the photolithography and copper electroplating of the inductor’s traces. The electrical parameters of the fabricated inductors were extracted using a pi-equivalent circuit and showed an average dc resistance of 29 mΩ, an inductance of 26 nH, and an ac resistance of 2.62 Ω at 100 MHz, which represents the targeted switching frequency of the system-in-package integrated voltage regulator. The organic substrate parasitic effects were accounted for through the extraction of an average shunt capacitance of 1.2 pF and an average parasitic conductance of 0.12 mS at 100 MHz. The measured 10% saturation current of the inductor was 9.6 A. The electrical parameters of the fabricated inductors were modeled and showed a good agreement with the measured data.

Index Terms—Integrated voltage regulators (IVRs), magnetic composite material, magnetic core, NiZn ferrite, package embedded solenoid inductor, system-in-package (SIP).

I. INTRODUCTION

INTEGRATED voltage regulators (IVRs) [1] provide on-package voltage regulation closer to the load, enabling faster power management loops with better power integrity and saving. Inductive IVRs require inductor integration. To reduce the inductor size for IVR miniaturization while significantly increasing the inductance density, the use of an integrated low-loss magnetic core inductor, switching at high frequency is required. Solenoid inductors [2], [3] can achieve a higher inductance density with reduced substrate parasitic losses (thus improved the overall IVR efficiency) compared to the planar racetrack [4] and single-via-winding [5] inductors due to confined parallel magnetic field lines to the substrate. Different processes have been developed for the fabrication of integrated magnetic core solenoid inductors, with on-silicon technology being dominant in the last decades. On-silicon magnetic core solenoid inductors having ferromagnetic (FM) [6]–[11], laminated multilayer (LM) [12]–[22], nanogranular (NG) [23], [24] and ferrite [25], [26] magnetic cores deposited using electroplating [6]–[8], [20], sputtering [9]–[11], [12]–[19], [23], [24], electroplating/dip-coating [21], thermal evaporation/folding [22], manual filling [25], spin spraying [26] and enclosed in polyimide [6], [10], [11], [15], [23], [24], [26], silicon oxide [7]–[9] or SU-8 [14], [20], [21] insulated, electroplated copper [15], [12]–[17], [23]–[25], sputtered aluminum [7], [8] windings/visas, or simply wire wound with a magnet wire [22] have been demonstrated. The FM inductors showed high-magnetic core losses resulting from their low resistivity, which make them unsuitable for high-frequency, high-efficiency IVRs. The multiple depositions [12]–[21], stiction (due to copper sacrificial layers etching) [20], [21], and delamination risks between the dielectric/metallurgical layers [12]–[21] and punching/wire winding [22] increase the LM inductors process complexity. Similarly, the multiple sputtering steps associated with the polyimide smoothness requirements [23], [24], the manual filling of the cavity [25], and the very low-core deposition rate [26] limit the core thickness while increasing the NG and ferrite inductors process cost/time. 

Other limitations of on-silicon inductors include silicon wafer brittleness and difficult processing as well as the high-LTCC firing temperature pose serious challenges for inductor and IVR integration. Compared to inorganic substrates, organic packages are a valuable option for inductors integration due to their low cost, low losses, low processing temperatures (<200 °C), and multilayer stacking/lamination capability. On-package NG core inductors were fabricated [31] by enclosing a sputtered NG film between the patterned bottom
and electroplated top copper windings covered with an organic dielectric layer and connected through laser-drilled copper vias. The inductors showed a limited core thickness with a rough printed wiring board (PWB) surface, which degrades the core permeability. On-package bondwire inductors [32], [33] were built by fully covering the aluminum bondwires in a manually brushed magnesium zinc (MgZn) ferrite composite [32], [33] or by assembling a laminated stack of Vitrovec 6155/dielectric tape and placing it between aluminum bondwires [34]. Although simple and relatively cost effective, the process [32]–[34] is limited by the bondwire size (diameter and thickness), material (aluminum and gold), and inter-windings separation due to the wirebonder head size. Moreover, the hand-brushed core deposition [32], [33] lacks precision and can damage the bondwire windings. As an alternative approach, we showed [35]–[37], [39] the advantages of a system-in-package (SIP) solution using package embedded magnetic core solenoid inductors with magnetic composite materials [37] for implementing a high-efficiency IVR. In this paper, a novel fabrication process of package embedded magnetic core solenoid inductors is demonstrated based on the previous design explorations [37], [39]. The process allows the deposition of a very thick magnetic core compared with [6]–[21], [23], and [24] using a simple and cost-effective printing process. An organic-substrate-compatible composite magnetic material [37] was used for the magnetic core to allow very good adhesion to the substrate with reduced built-in stress at the core–substrate interface. The good dielectric properties of the composite material [37], [40], [41] avoid the use of an insulation layer at the core/windings interface, which simplifies the process and reduces its overall cost/time. Moreover, the process takes the advantage of the printed core shape to deposit the inductor’s top windings while simultaneously interconnecting them to the inductor’s bottom windings without vertically patterned vias after successive planarization/photolithography steps [6]–[8], [10]–[17], [20], [2]–[24], [26], [28]–[30]. This also simplifies considerably the process compared with [6]–[8], [10]–[17], [20], [2]–[24], [26], and [28]–[31] while reducing significantly the dc resistance resulting from the contact resistance at the vias/windings interface. The rest of this paper is organized as follows. In Section I, the design/modeling procedure of the inductors is presented. In Section III, the fabrication process of the inductors is discussed in detail. The characterization results of the fabricated inductors are provided in Section IV and compared with the simulation results.

II. DESIGN AND MODELING

The goal was to design embedded solenoidal inductors for a four-phase SIP buck converter [36], [37], [39] with a minimum inductance of 25 nH/phase at a 100 MHz switching frequency [39]. The 3-D solenoid inductors [Fig. 1(a)] were designed with a magnetic core enclosed in copper windings, built on the top side of a two-copper-layer FR4 PWB (70 μm-thick copper for each side and 500 μm-thick FR4 substrate). The top copper layer was used to define the inductor bottom windings, which were covered with the magnetic core, and the contact pads for the top copper windings. The bottom copper layer was used as a ground plane for the electromagnetic interference reduction. A NiZn ferrite epoxy composite magnetic material having good insulation properties combined with a relatively high-permeability and low-electromagnetic losses at high frequency was chosen as the core material [37]. Consequently, no insulation layer between the magnetic core and the copper windings [40], [41] was used in the designed inductor compared with the structure in [39]. Moreover, the dome-like magnetic core shape resulting from the stencil printing deposition process was also considered in the design instead of a rectangular core [39] by using experimentally measured core profiles in the simulations to accurately model the inductors. The design parameters of the inductors were the magnetic core thickness $t_{mag\_core}$, length $l_{mag\_core}$, width $W_{mag\_core}$, number $N$, and width $W_{trace}$ of the copper windings while the overall area $A$ and the windings thicknesses were kept fixed. A 3-D model of the solenoid inductor of Fig. 1(a) was created in a full-wave simulator (Ansys Electronics Desktop ver. 2015.2) to account for the complex electromagnetic field distributions and loss effects in the magnetic core and the copper windings. The measured complex permeability spectrum of the NiZn ferrite magnetic material [37], was used into the solver to accurately represent the magnetic core. The simulations were run from 10 MHz to 1 GHz, and the results were extracted as frequency-dependent two-port network parameters (S-parameters) and converted into a simple pi-equivalent circuit, as shown in Fig. 1(b), where the series inductance $L$ and resistance $R_{ac}$ represent the inductor’s effective inductance and losses, respectively, while the parallel conductance and capacitance represent the inductor’s parasitics due to the organic substrate and the copper ground plane A pi-topology is a simple and an acceptable representation of the inductor since the targeted switching frequency of the IVR (100 MHz) is below the first self-resonant frequency of the inductor (>1 GHz), and consequently, the impedance is
The dc resistances $R_{dc}$ of the designed inductor was obtained in Ansys Maxwell ver.2015.2. The extracted inductor electrical parameters ($R_{dc}$, $L$, and $R_{ac}$) were used as inputs to evaluate the impact of the inductor on the overall IVR efficiency, following the same analytical approach (based on the small-ripple approximation representing the inductor current as a triangular waveform) described in [34] and [37] which considers all the major loss components from the buck chip, the passives (inductor and output capacitor), and power delivery network. Based on the overall IVR peak efficiencies (at optimum load) evaluation, multiple cycles of simulation and modification of the inductor design parameters were carried out [Fig. 1(b)] until the highest overall IVR efficiency was obtained for a given inductor geometry with an inductance close to 25 nH. The inductor design approach is summarized in Fig. 1(b). The extracted RF parameters and the dimensions of the final inductor design are shown in Fig. 2 and Table I, respectively, where an inductance of 27.8 nH was obtained at 100 MHz, which represents a $5 \times$ inductance density increase compared to an air core inductor of the same size. Based on the dimensional parameters of the magnetic core and the inductor (Table I), the organic substrate (PWB) for the inductor fabrication and the stencil for magnetic core deposition (Fig. 3) were designed in Cadence and AutoCAD, respectively. The PWB design included two patterns of the bottom copper windings connected to SMA pads with feedlines as well as process alignment marks. Thru–reflect–line (TRL) deembedding structures were also designed for the electrical characterization of the inductors. The stencil design had two openings for magnetic core printing and alignment marks for precise alignment with the PWB.
TABLE I
DIMENSIONAL PROPERTIES AND MAIN FIGURES OF MERIT (AT 100 MHZ) OF THE DESIGNED INDUCTOR (A COMPARISON TO AN AIR CORE INDUCTOR OF SIMILAR SIZE IS INCLUDED.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>$I_{mag}$</th>
<th>$w_{mag}$</th>
<th>$A_{ind}$</th>
<th>$w_{copper}$</th>
<th>$w_{seed}$</th>
<th>$N$</th>
<th>$A$</th>
<th>$R_{DC}$</th>
<th>$L/(L_{ind})$</th>
<th>$R_{AC}$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mag core</td>
<td>4064</td>
<td>1827</td>
<td>3097</td>
<td>300</td>
<td>70</td>
<td>500</td>
<td>200</td>
<td>6</td>
<td>11.56</td>
<td>10.2</td>
<td>27.8</td>
</tr>
<tr>
<td>Air core</td>
<td>4064</td>
<td>1827</td>
<td>3097</td>
<td>300</td>
<td>70</td>
<td>500</td>
<td>200</td>
<td>6</td>
<td>11.56</td>
<td>10.2</td>
<td>5.19</td>
</tr>
</tbody>
</table>

Fig. 4. Fabrication process flow of the solenoid inductors. (a) Initially two-copper layer, FR4 PWB substrate. (b) PWB etching to define the bottom copper tracks. (c) Stencil printing of the NiZn ferrite magnetic core. (d) Photoresist deposition and patterning using photolithography. (e) Sputter deposition of a seed layer of 50 nm Cr + 200 nm Au. (f) Liftoff process to remove the photoresist and pattern the seed layer for the top windings electroplating. (g) Photoresist deposition and patterning using photolithography. (h) Electrodeposition of the top copper windings. (i) Removal of the photoresist. (j) Photoresist deposition and patterning using photolithography. (k) Seed layer and photoresist removal.

III. EXPERIMENT

The fabrication process flow of the solenoid inductor is shown in Fig. 4. A 640 μm thick, two-copper layer FR4 PWB (70 μm thick for both copper layers and 500 μm-thick FR4 layer) was used as a substrate Fig. 4(a). First, the bottom inductor windings on the top side of the substrate were defined using the standard PWB copper etching process Fig. 4(b). The copper traces, width, separation, and thickness were measured using an optical microscope and the Veeco Dektak 150 surface profilometer and were found to be around 450 μm, 225 μm [Fig. 5(a)], and 74 μm [Fig. 5(c)], respectively. Then, the magnetic core was deposited on the top of the bottom copper windings Fig. 4(c) by stencil printing a custom prepared FR4 compatible composite magnetic paste, made by mixing a magnetic powder (FP350 NiZn ferrite from pptechnology) with an epoxy polymer at 85 wt% [36] using the MPM SPM 7279 Semiautomatic Stencil Printer (PPM Inc.). The substrate was cured for 1 h at 180 °C to form the magnetic composite core as shown in Fig. 5(b). The cured core showed no reaction to commonly used solvents, a very strong adhesion to the substrate, and good dielectric properties [36] assessed by a measured very high dc resistance (beyond 30 MΩ) which avoided the use of insulation layers between the magnetic core and the copper windings [40], [41].

The measured profile of the magnetic core is shown in Fig. 5(c), where the average measured core thickness is around 350 μm. After the magnetic core deposition, a first photolithography step was used to pattern a seed layer on the top of the magnetic core for the electroplating of the top windings. A thick photoresist mold (>74 μm which is the bottom windings thickness) was required to ensure the full coverage of the inter-pads space of the bottom copper windings with photoresist. Intervia 65A BPN photoresist was spray coated directly on the top of the magnetic core and the bottom copper windings using the Suss Delta Alta Spray coater. A photoresist thickness of 100 μm was obtained, and no softbaking was applied to avoid trapped air bubbles in the photoresist mold. The photoresist was exposed using the non-contact lithography mode of the EVG 620 Mask Aligner at 365 nm wavelength and 5 mW/cm² for 200 s. The exposed photoresist was then developed in RD6 developer for 5 min Fig. 4(d). A 50 nm chromium/200 nm gold seed layer was then sputtered at 5 mtorr using the Unifilm multisource sputtering system at a rate of 8.3 and 33 A/s for chromium and gold, respectively, Fig. 4(e). A liftoff process [Fig. 4(f)] was used to pattern the seed layer and remove the photoresist Fig. 5(d). A second photolithography step Fig. 4(g) similar to the previous photolithography step was required to fabricate the photoresist mold for the top windings electroplating. A 170 μm-thick Intervia 65A BPN photoresist was spray coated directly on the top of the patterned seed layer to allow the deposition of very thick copper windings to reduce the dc resistance of the inductor. The photoresist was exposed for 330 s and then developed in RD6 for 8 min. The top copper windings were then electroplated Fig. 4(h) using an acid copper-based electroplating bath at a current density of 10 mA/cm² for a plating time of 6 h. The photoresist mold was then removed in acetone solvent Fig. 4(i). A third photolithography step was required to protect the plated top copper windings from the seed layer etching solutions. An 8 μm-thick AZ 4620 photoresist was spray coated on the top of the inductor, softbaked for 2 min at 120 °C, and exposed for 100 s. The photoresist was then developed in RD6 for 4 min Fig. 4(j). The seed layer was removed Fig. 4(k) using standard gold and chromium etching solutions from Sigma-Aldrich. Finally, the AZ 4620 photoresist was removed in acetone Fig. 4(i). An example of a fabricated inductor is shown in Fig. 5(e). A measured profile of the electroplated copper top windings is shown in Fig. 5(f) where around 76.5 μm-thick copper was deposited on the top of the magnetic core. The inductors’ dc resistance was measured using the four wires mode of the HP 34401A multimeter. The RF parameters of the inductors...
were characterized between 20 MHz and 1 GHz using the Agilent H8363B Vector Network Analyzer. A standard SOLT calibration was carried out, followed by the measurement of the two port S-parameters of the inductors and the TRL deembedding structures which were then mathematically post-processed to extract the effective inductors RF parameters.

**IV. RESULTS AND DISCUSSION**

Different inductors were characterized and showed an average dc resistance of 29 mΩ while the inductance varied from 25.64 to 31 nH (at 100 MHz) which corresponds to an
average value of 28.32 nH with ±3.32 nH deviation from the targeted minimal 25 nH inductance. Fig. 6 shows an example of the extracted RF parameters of an inductor. The inductance decreased due to the permeability decrease of the NiZn ferrite composite beyond its ferromagnetic resonance frequency [36] while the ac resistance increased, resulting from the pronounced magnetic core and RF (proximity and eddy current) losses at high frequency. The inductor showed a quality factor $Q$ of 6.37 at 100 MHz with a maximum of 11.33 at 41.1 MHz [Fig. 7(a)]. The inductor models (section) were updated based on the measured dimensions of the fabricated inductors (Table II), and the simulation results were compared with the experimentally measured RF parameters as shown in Fig. 6 and summarized in Table III. A good match is observed between the experimental and modeling results. The discrepancies observed for $C_2$, $G_2$, and $R_{ac}$ (beyond 300 MHz) could be attributed to errors resulting from the deembedding process which was carried out using deembedding structures defined on a separate board. Moreover, the used pi-model assumed an ideal two-port inductor model, which implies perfectly symmetric ports (thus $C_{1\_sim} = C_{2\_sim}$ and $G_{1\_sim} = G_{2\_sim}$), which was not the case for the fabricated inductors due to the fabrication process (printed core and windings definition) and the deembedding procedure which explains the differences observed between $C_2$, $G_2$ and $C_{2\_sim}$, $G_{2\_sim}$, respectively. The effect of the dc current on the inductance is shown in Fig. 7(b), where 1.94 nH decrease is observed for 6 A at 41.1 MHz which corresponds to a 6.2% drop from the unbiased initial inductance value. The 10% saturation current of the inductor is estimated accordingly to be around 9.6 A (at maximum $Q$), which is higher than the targeted maximum load current for the IVR (2.5 A/phase).

### V. Conclusion

The SIP-based IVRs represent a valuable approach to achieve combined high-integration density and efficiency for the point-of-load voltage regulation. In this paper, a novel on-package magnetic core solenoidal power inductor was demonstrated for the implementation of a high efficiency, 100 MHz switching SIP-based buck-type IVR. The optimum inductor design was selected based on the highest achievable overall IVR efficiency. The inductor was fabricated on an organic substrate using stencil printing and non-contact lithography processes. A pi-equivalent circuit and standard TRL deembedding were used for the inductor characterization, and a good match was obtained with the modeling results. The developed fabrication process will be used for the integration of package embedded magnetic core solenoidal power inductors in both single phase and four phase SIP-based IVRs allowing three voltage conversion ratios (5 V:1 V, 3 V:1 V, and 1.7 V:1 V).

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